CS2100 Computer Organisation

Tutorial #8: MSI Components

(Week 10: 25 – 29 March 2024)

Answers to Selected Questions

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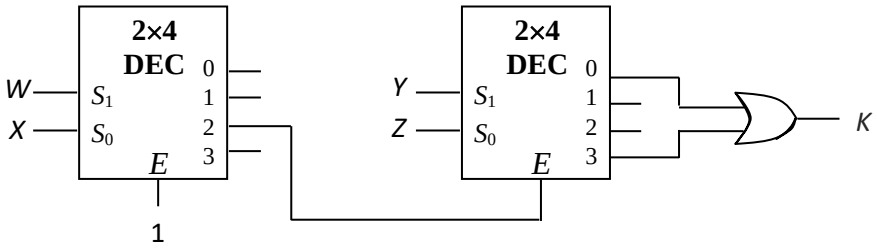
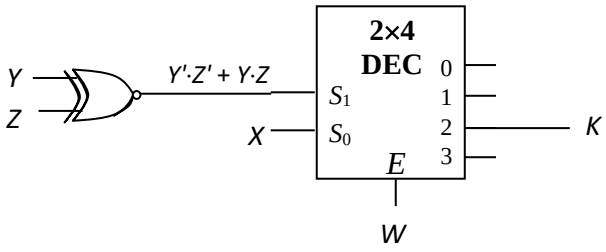
2. You are given the following Boolean function: ***K(W,X,Y,Z)*** **= Σ*m*(8, 11)**.

   You are to implement this function using the fewest number of one-enabled 2×4 decoder with normal outputs and at most one logic gate? (Logic gates, as you have learned, are NOT, AND, OR, NAND, NOR, XOR, and XNOR.)

   The following is one solution. Is there a simpler circuit using just one decoder and one logic gate?



Answer: There might be other answers.



3. [AY2011/2 Semester 2 Exam question]
You are to design a converter that takes in 4-bit input *ABCD* and generates a 3-bit output *FGH* as shown in Table 1 below.

Input				Output		
A	***B***	***C***	***D***	***F***	***G***	***H***
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Table 1

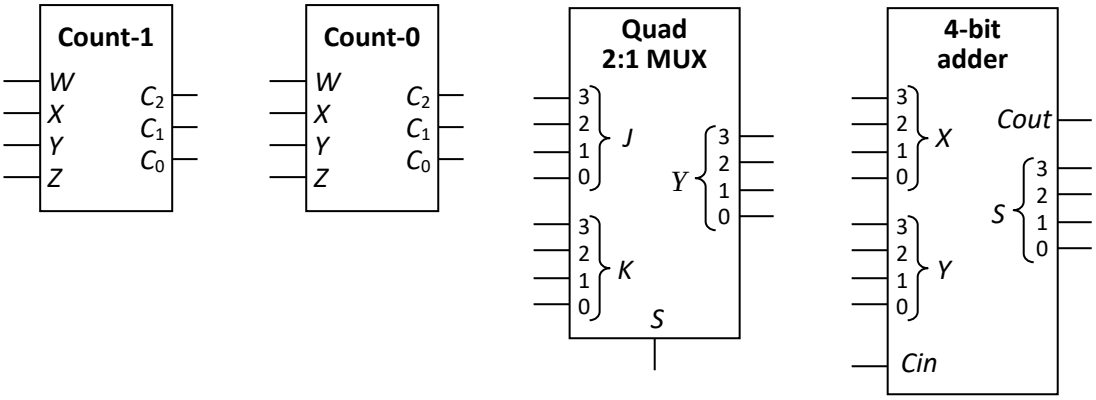
S	$Y_3Y_2Y_1Y_0$
0	$J_3J_2J_1J_0$
1	$K_3K_2K_1K_0$

Table 2

You are given the following components:

a. A **Count-1** device that takes in a 4-bit input *WXYZ* and generates a 3-bit output $C_2C_1C_0$ which is the number of 1s in the input. For example, if *WXYZ* = 0111, then $C_2C_1C_0$ = 011 (or 3).
b. A **Count-0** device that takes in a 4-bit input *WXYZ* and generates a 3-bit output $C_2C_1C_0$ which is the number of 0s in the input. For example, if *WXYZ* = 0111, then $C_2C_1C_0$ = 001 (or 1).
c. A **quad 2:1 multiplexer** that takes in two 4-bit inputs $J_3J_2J_1J_0$ and $K_3K_2K_1K_0$, and directs one of the inputs to its output $Y_3Y_2Y_1Y_0$ depending on its control signal *S*, as shown in Table 2 above.
d. A **4-bit parallel adder** that takes in two 4-bit unsigned binary numbers and outputs the sum.

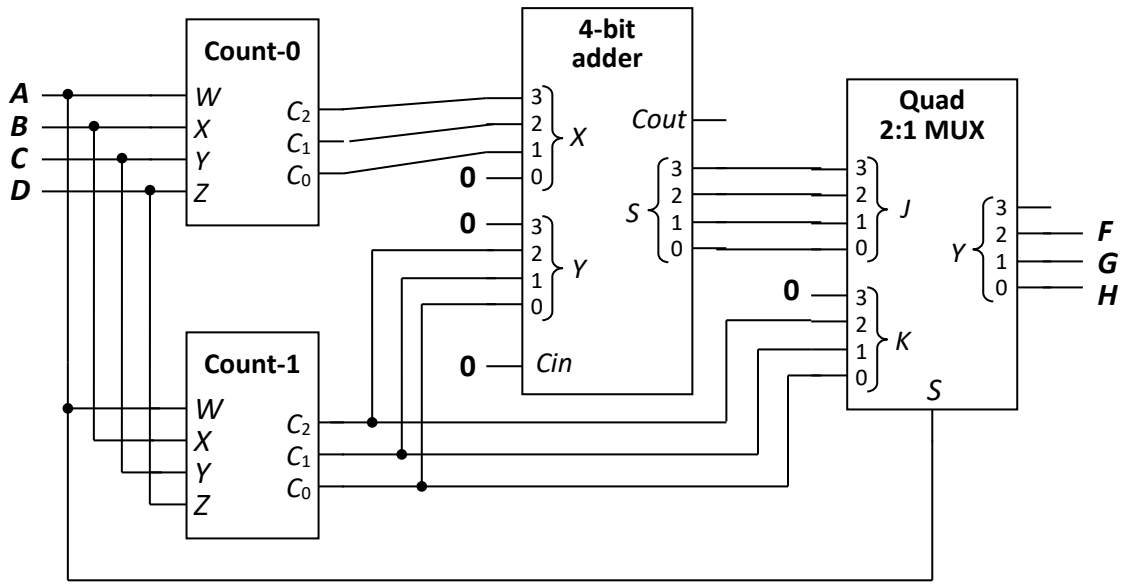
The block diagrams of these components are shown below:



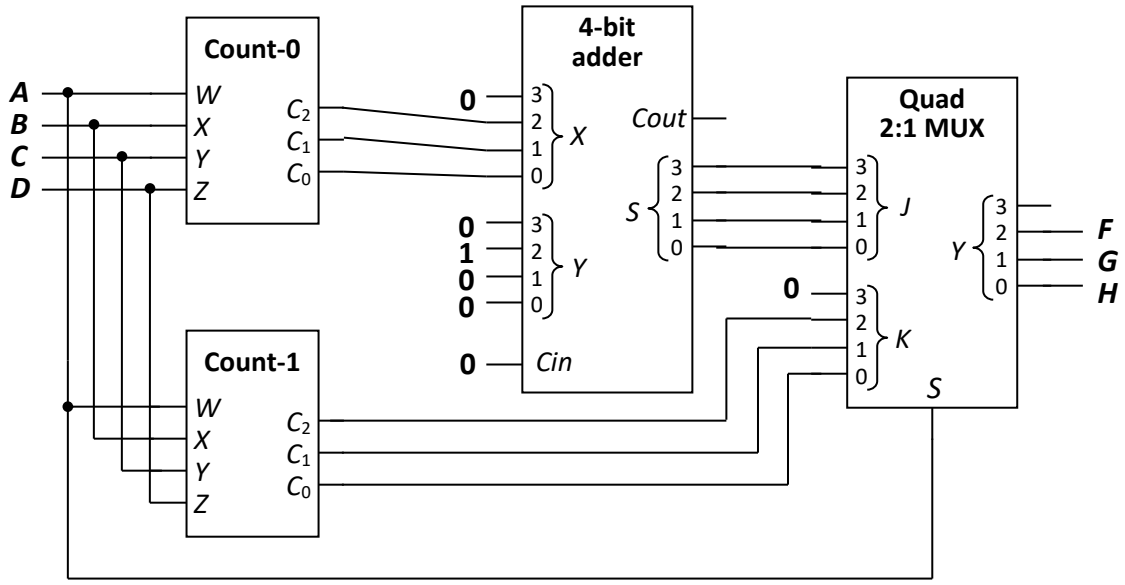
Given the above 4 components, you are to employ block-level design to design the converter, <u>without using any additional logic gate or other devices</u>. You may observe that if *A* = 1, then the output *FGH* is simply the number of 1s in the input *ABCD*. You are to make your own observation for the case when *A* = 0.

[Hint (not given in exam): You need only use one of each of the components. Complete the diagram below.]

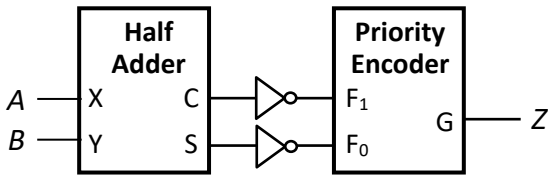
Key ideas:
1. If *A* = 1 (or *D* = 0), count #1s in *ABCD*.
2. If *A* = 0 (or *D* = 1), either
   a. #1s + 2 × #0s; or
   b. 4 + #0s


A
B
C
D
Count-0
W
X
Y
Z
C2
C1
C0
Count-1
W
X
Y
Z
C2
C1
C0
4-bit adder
3
2
1
0
X
0
0
3
2
1
0
Y
0
Cin
Cout
S
3
2
1
0
Quad 2:1 MUX
3
2
1
0
J
0
3
2
1
0
K
S
Y
3
2
1
0
F
G
H

OR


A
B
C
D
Count-0
W
X
Y
Z
C2
C1
C0
Count-1
W
X
Y
Z
C2
C1
C0
4-bit adder
0
3
2
1
0
X
0
1
0
0
3
2
1
0
Y
0
Cin
Cout
S
3
2
1
0
Quad 2:1 MUX
3
2
1
0
J
0
3
2
1
0
K
S
Y
3
2
1
0
F
G
H

4. [AY2023/24 Semester 1 Exam]
A Boolean function $Z(A,B)$ is implemented using a half adder, two inverters, and a 2-to-1 priority encoder as shown below. The function tables of the half adder and priority encoder are also shown below.



Half adder

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Priority encoder

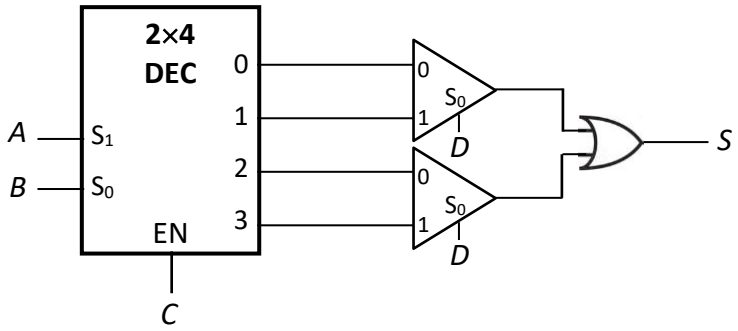
F_1	F_0	G
0	0	X
0	1	0
1	X	1

The circuit above may be replaced by a single 2-input logic gate. What is the logic gate?

Answer: NAND gate

X	Y	C	S	F_1	F_0	G
0	0	0	0	1	1	1
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	1	0	0	1	0

5. [AY2023/24 Semester 1 Exam]
A Boolean function $S(A,B,C,D)$ is implemented with a 2×4 decoder with one-enable, two 2:1 multiplexers and an OR gate as shown below.



What is $S(A,B,C,D)$ in Σm notation?

Answer:

$S(A,B,C,D) = \Sigma m(\mathbf{2,7,10,15})$.

$S = (D' \cdot (C \cdot A' \cdot B') + D \cdot (C \cdot A' \cdot B)) + (D' \cdot (C \cdot A \cdot B') + D \cdot (C \cdot A \cdot B))$
$= A' \cdot B' \cdot C \cdot D' + A' \cdot B \cdot C \cdot D + A \cdot B' \cdot C \cdot D' + A \cdot B \cdot C \cdot D$
$= m2 + m7 + m10 + m15$