

Abhik Roychoudhury
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Research Interests

Software and System Validation, Predictable System Design with focus on Embedded Systems.

Education

- Ph.D. Computer Science (2000), State Univ. of New York (SUNY) at Stony Brook (USA).
 - *Dissertation*: Program Transformations for Verifying Parameterized Systems.
 - *Supervisors*: I.V. Ramakrishnan and C.R. Ramakrishnan.
- M.S. Computer Science (1997), State Univ. of New York (SUNY) at Stony Brook (USA), GPA: 3.96/4.
- B.E. Computer Engineering (1995), Jadavpur University (India), GPA: 5.00/5.
 - 1st rank in Engineering Faculty in freshman/sophomore years (1991-1993).
 - 2nd rank in Engineering Faculty in junior/senior years (1993-1995).

Employment

- Since July 2007: Associate Professor (with Tenure), School of Computing, National University of Singapore.
- 2001 - 2007: Assistant Professor (Tenure-track), School of Computing, National University of Singapore.
- 1995 - 2000: Research and Teaching Assistant, Department of Computer Science, State University of New York (SUNY) at Stony Brook.

Visiting Appointments

- 2008: Visiting Researcher, Microsoft Research (5 months - sabbatical leave from NUS).
- 2007: Visiting Faculty, Department of Computer Science and Automation, Indian Institute of Science, Bangalore (2 months).
- 1998: Member of Technical Staff, Bell Laboratories, Lucent Technologies, New Jersey (3 months).
- 1997: Course Instructor, Department of Computer Science, SUNY at Stony Brook (2 months).

Funded Research Projects

- As Principal Investigator (PI)

- *Symbolic Taint Analysis*, PI, Funded by Defense Science and Technology Agency (DSTA), 2009-2012 (3 years), S\$397,290.
 - *Timing Analysis of Behavioral System Models*, PI, Funded by NUS University Research Council (URC), October 2007 - 2010 (3 years), S\$ 250,000.
 - *Tools and techniques for Model based Software Debugging*, PI, Funded by Agency of Science Technology and Research (A*STAR), September 2004 - 2007 (3 years), S\$362,000.
 - *Correctness and Performance Issues in the CLI memory model*, PI, a small grant funded by Microsoft for one year (2005-2006), US\$15,000.
 - *Efficient Design Space Exploration of Embedded Systems*, PI, Funded by InfoComm and InfoTech Initiative (ICITI) at NUS, July 2003 - 2006 (3 years), S\$75,000.
 - *Protocols for System-on-chip Designs*, PI, Funded by Faculty Research Council (internal grant), Oct 2001 -2004 (3 years), S\$38,800.
 - *Formally Verifying Safety Properties of Distributed Systems*, PI, Funded by Faculty Research Council (internal grant), April 2001 -04 (3 years), S\$29,500.
- As Co-Principal Investigator (Co-PI)
 - *EASEL: Engineering Architectures and Software for the Embedded Landscape*, Co-PI, Funded by Agency of Science Technology and Research (A*STAR), March 2006-09, S\$1.4 million.
 - *Formal Design Techniques for Reactive Embedded Systems*, Co-PI, Funded by Agency of Science Technology and Research (A*STAR), March 2003 - 2006 (3 years), S\$429,000.
 - *Techniques to Support Timing and Power Guarantees for Embedded Code*, Co-PI, Funded by University Research Council (URC) of NUS, July 2003 - 2006 (3 years), S\$231,000.
 - *Model-based Approach to Integrated Timing Analysis of Embedded Systems*, Co-PI, Funded by Faculty Research Council (internal grant), March 2007-08 (1 year), S\$ 41,000.
 - *Reactive Embedded Systems: High-level Design Methods*, Co-PI, Pilot project funded by Agency of Science Technology and Research (A*STAR), Nov 2001 - 02 (1 year), S\$ 29,000.

Honors and Awards

- ACM SIGSOFT Distinguished Paper Award (from ESEC-FSE 2009).
- IBM Faculty Award, 2008.
- Tan Kah Kee Young Inventor's Award, Silver Award in Open Section, for building the Java program debugging and comprehension tool JSlice, 2008.
- Best paper award nomination from
 - ACM Design Automation Conference (DAC) 2009.
 - International Conference on Hardware Software Codesign and System Synthesis (CODES-ISSS) 2008.
 - 19th Euromicro Conference on Real-time Systems (ECRTS) 2007.
- Award from ACM SIGPLAN Professional Activities Fund, 1999.
- Top score in the Ph.D. Qualifier Examination, Department of Computer Science, State University of New York at Stony Brook, 1996.

- Award and Medal for 1st rank in Engineering Faculty, Jadavpur University (India) in freshman and sophomore years (1991-1993), and 2nd rank in Engineering Faculty, Jadavpur University (India) in junior and senior years (1993-1995).
- National Scholarship and Award for ranking 8th among all candidates in Higher Secondary Education (equivalent of A levels) in the state of West Bengal, India, 1991.
- Ranked 2nd among all candidates in the West Bengal Joint Entrance Examination for admission to Engineering colleges/institutes in the state of West Bengal, India, 1991.

Teaching Experience

- Written a textbook for senior undergraduate courses, entitled “*Embedded Systems and Software Validation*”. The book has been published by Elsevier (formerly Morgan Kaufmann) Systems-on-Silicon series in 2009.
- Taught various courses at NUS in both undergraduate and graduate levels.
 - CS 4271 *Critical Systems and their Verification*
Designed this undergraduate course on system modeling and verification, focusing on model checking
 - CS 4272 *Hardware Software Codesign*
Covers Modeling, Hardware-Software Partitioning, Software Analysis, Compilation and Hardware Platforms. I made substantial changes in the course contents.
 - CS 5219/6214 *Automated Software Validation*
Proposed and designed this graduate course in software validation which studies model checking, theorem proving and their combinations.
 - CS 2104 *Programming Language Concepts*
This is a first course on principles of programming languages that I taught twice — in 2001-02 and 2002-03.
 - CS 1102 *Data Structures and Algorithms*
This is a first course in data structures and programming that I taught in 2000-01.
- Taught a graduate course on Software Validation while visiting Indian Institute of Science (IISc) in May - July 2007.
- Actively involved in designing and formulating the new *written Ph.D. Qualifier Examination* at NUS School of Computing. Currently serving as the *coordinator* of CS5201, the PhD Qualifier Examination in Theoretical Computer Science. Details about the exam appear in <http://www.comp.nus.edu.sg/~abhik/CS-QE>
- Contributed article on education/pedagogy based on experience in teaching courses on formal verification.
 - “Introducing Model Checking to Undergraduates” by Abhik Roychoudhury, In Formal Methods Education Workshop 2006 (co-located with Formal Methods Symposium (FM) 2006). The paper is available from <http://www.comp.nus.edu.sg/~abhik/pdf/fm-ed06.pdf>

Graduate Student Supervision and Mentoring

- *PhD student Supervision (Current)*

- Lei Ju, Ph.D. student (Since August 2005), Co-supervised with Samarjit Chakraborty, *Debugging Timing Properties of MSC-based System Models*.
 - Bach Khoa Huynh, Ph.D. student (since January 2008).
 - Dawei Qi, Ph.D. student (since August 2008), Debugging of Evolving Programs
 - Sudipta Chattopadhyay, Ph.D. student (since January 2009), Software timing analysis for multi-cores.
- *Past PhD students*
 - Ankit Goel, Ph.D., Sole supervision, *Parameterized Validation of MSC-based System Models*, Moved to: INRIA.
 - Vivy Suhendra, Ph.D. (graduated 2009), Co-supervised with Tulika Mitra, *Memory Optimizations for Developing Predictable Embedded Software*, Awarded *Microsoft Research Asia Fellowship* for her work in 2006-07. Moved to: Institute of Infocomm Research (I2R) Singapore.
 - Tao Wang, Ph.D. (graduated Feb 2008), Sole Supervision, *Bytecode level Dynamic Analysis for Software Debugging*, Adjudged **Best PhD thesis** from School of Computing in 2007-08, Awarded *Microsoft Research Asia Fellowship* in 2004-05, also awarded *Presidential Graduate Fellowship* by NUS. Moved to: Morgan Stanley.
 - Xianfeng Li, Ph.D. (graduated Dec 2005), Co-supervised with Tulika Mitra, *Micro-architectural modeling for Timing Analysis of Embedded Software*, Awarded *Dell Fellowship*, *Dean's Graduate Award* during his PhD study at NUS. Moved to: Peking University.
 - *Past Post-doctoral Fellows*
 - Dr. Sun Meng, Ph.D. Beijing University China (05). Worked in 2005-06.
 - Dr. Adrian Curic, Ph.D. VERIMAG France (06). Worked in 2007.
 - *Past M.Sc. Students*
 - Liang Guo, (Graduated 2008), Sole supervision, *Debugging Statechart Models via Model-code Traceability*, First Employment: CreditSuisse, Singapore.
 - Tuan-Anh Tran, M.Sc. (Graduated 2005), Co-supervised with P.S. Thiagarajan, *Protocol Converters from Scenario-based Specifications*, First Employment: Friar Tuck Pte Ltd (Singapore).
 - Qinghua Shen, M.Sc. (Graduated 2004), Co-supervised with Tulika Mitra, *Multi-threaded Java from Multi-processor Perspective*, First Employment: Creative Technology Ltd (Singapore).
 - Hemendra Singh Negi, M.Sc. (Graduated 2004), Co-supervised with Tulika Mitra, *Two Concrete Problems in Worst-Case Execution Time Analysis*, First Employment: Mentor Graphics, New Delhi (India).
 - Lei Xie, M.Sc. (Graduated 2003), Sole supervision, *Performance Impact of Multithreaded Java Semantics on Multiprocessor Memory Models*.
 - *PhD/M.Sc. Thesis Committees:*
 - PhD thesis evaluator of several PhD students from NUS — Andrew Edward Sentosa, Corneliu Popeea, Sun Jun, Hamid Abdul Basit, Chen Chunqing.
 - Thesis committee member of several M.Sc. students from NUS — Xu Na and Kamrul Hasan Talukder.

- External Assessor of the following PhD thesis – “A formal framework for a service oriented multi-agent society” by Manas Ranjan Patra (University of Hyderabad, India).

Undergraduate Student Supervision

- S.R. Karri, *Verification of AMBA bus protocol*, graduated 2002. This work led to a publication in Design Automation and Test in Europe Conference (DATE) 2003.
- S.C. Choudhary, *Symbolic simulation of Live Sequence Charts*, Co-supervised with Roland Yap, graduated 2003. This work led to a publication in the Intl. Conf. on Practical Applications of Declarative Languages (PADL) 2004.
- Jia Zhan, *Multi-threaded Java from Multi-processor perspective*, Co-supervised with Tulika Mitra, graduated 2003.
- K.K. Subramanian, *Extending algorithmic searches for Design Space Exploration of Embedded Systems*, graduated 2004.
- Lei Ju, *Tracing methods to help multi-threaded program debugging*, graduated 2005.
- Xue Luo, *A Play-in front-end to a Live Sequence Chart symbolic simulator*, graduated 2005.
- Mustafa Yuceabdali, *Search optimizations for model checking of C# programs*, graduated 2006.
- Chong Tat Chua, *Improved instrumentation methods for software fault localization*, graduated 2006.
- Shek Chian Low, *Verification of Interacting Process Classes using PVS prover*, graduated 2007.
- Kelly Tan, *Verification of Live Sequence Charts using PVS prover*, graduated 2007.
- Wei Chern Choo, *Explanation of counter-examples in SPIN for education purposes*, currently supervising.

Patent

- “Methods and apparatus for generating a verified algorithm for transforming a program from a first form to a second form”, United States Patent 6,343,372, Awarded: January 29, 2002. Co-Inventors: Amy P. Felty and Douglas J. Howe, Assignee: Lucent Technologies Inc. (USA).

Software Tools released

- *Jslice, a dynamic slicing tool for debugging Java programs.*
Dynamic slicing is a popular and well-known software analysis technique. It is useful for program debugging as well as comprehension of program functionality/performance. It can also be integrated as a module in many software validation tools (such as software model checkers). Slicing can explain the reasons for unexpected variable values in a program execution, by analyzing control and data dependencies. To the best of our knowledge, prior to our work no dynamic slicing tool was available for Java programs. The Jslice tool resulted from the following research paper.
 - Using Compressed Bytecode Traces for Slicing Java Programs, by Tao Wang and Abhik Roychoudhury, Intl. Conf. on Software Engineering (ICSE) 2004.

The JSlice tool can be downloaded from <http://jslice.sourceforge.net/>
Its current user base includes over 150 different research/industrial groups spread over 30 different countries.

- *Chronos, a Worst-case Execution Time (WCET) analysis tool for C programs.*
Estimating the maximum execution time of a program is a generic problem. To obtain such estimates tightly, one needs to analyze the program flow as well as the the timing effects of the underlying processor micro-architecture. Such execution time estimates are directly useful for scheduling of hard real-time systems as well as in other applications (like guiding program optimizations). Our execution time analysis tool resulted from several research papers, including the core modeling which was reported in the following.
 - Modeling Out-of-order Processors for WCET Analysis, by Xianfeng Li, Abhik Roychoudhury and Tulika Mitra, Real-Time Systems Journal 2006, Preliminary version published in IEEE Real-time Systems Symposium (RTSS) 2004.

The tool is available from <http://www.comp.nus.edu.sg/~rpembed/chronos>
Its current user base includes over 85 different research groups in 16 different countries.

Invited Talks and Tutorials

- “Debugging as a Science, that too, for Evolving Programs”, Keynote given at *3rd International Workshop on Harnessing Theories for Tool Support in Software (TTSS) 2009*, a workshop held along with the *International Colloquium on Theoretical Aspects of Computing (ICTAC) 2009*, August 2009, Venue: Kuala Lumpur, Malaysia.
- “Synthesis of Scenario-based System Models”, Invited Presentation at the Track on Highly Reliable Software at the *International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (ISoLA)*, November 2006, Venue: Paphos, Cyprus.
- “Interacting Process Classes”, Talk given at the Workshop on Predictable Software Component Assembly, Organized by *University of Manchester*, Manchester (UK), September 2005, and at the Workshop on Formal Methods for Design and Analysis of Software, Organized by *Microsoft Research*, Bangalore (India), October 2005.
- “Scenario based methods for system design” Invited tutorial (jointly with P.S. Thiagarajan) at *International Conference on Application and Theory of Petri Nets and Other Models of Concurrency (ICATPN)*, June 2005, Miami (USA).
- “Automated Generation of Protocol Converters from Scenario-based Specifications”, *Workshop on Predictable Software Component Assembly*, Sponsored by CoLogNet (the European Network for Excellence in Computational Logic), May 2004, Venue: Manchester, UK.
- “Program Transformations for Automated Verification” Invited tutorial (jointly with I.V. Ramakrishnan) at *International Conference on Logic Programming (ICLP)*, August 1 2002, Copenhagen (Denmark).
- “Induction Proofs for Verification of Parameterized Systems”, Post-conference workshop on Infinite State Systems for Intl. Conf. on Foundations of Software Technology and Theoretical Computer Science (FST&TCS) 2001, Chennai (India), December 2001.

Research Citations as of 2009

- *Total number of citations = 800+*
All citation data has been collected from Google Scholar.
- *h-index = 17.* *h-index* is the maximum value of *h* such that there are *h* papers co-authored by me with *h* or more citations.

Book

- “Embedded Systems and Software Validation”, Abhik Roychoudhury, *Elsevier, 2009.*

Invited Papers published as Book chapters

- “Worst-case Execution Time and Energy Analysis”, Tulika Mitra and Abhik Roychoudhury, *The Compiler Design Handbook, Y.N. Srikant and Priti Shankar Editors, CRC Press, To appear.*
- “Unfold/fold Transformations for Automated Verification of Parameterized Concurrent Systems”, Abhik Roychoudhury and C.R. Ramakrishnan, *Invited chapter in a book ”Program Development in Computational Logic”, Editors Maurice Bruynooghe and Kung-Kiu Lau, Springer Verlag, LNCS 3049, 2004, pages 262-291.*
- “Communicating Transaction Processes: An MSC-Based Model of Computation for Reactive Embedded Systems”, Abhik Roychoudhury and P. S. Thiagarajan, *Lectures on Concurrency and Petri Nets, Springer Verlag, LNCS 3098, pages 789-818, 2003.*

Full Publication List (Journals, Conferences)

(*Non-exhaustive list — post-Ph.D. publications are grouped into two related areas. Acceptance rates of conference papers are marked wherever this data is known. All papers are full-length papers unless indicated otherwise.*)

- **Software Modeling and Validation**

- **[ESEC-FSE’09]** “DARWIN: An Approach for Debugging Evolving Programs ”, Dawei Qi, Abhik Roychoudhury, Zhenkai Liang, Kapil Vaswani *Joint meeting of ESEC and ACM SIGSOFT Symposium on the Foundations of Software Engineering (FSE), ESEC-FSE 2009, ACM SIGSOFT Distinguished Paper Award, Acceptance rate = 32/217.*
- **[FM’09]** “Fair Model Checking with Process Counter Abstraction”, Jun Sun, Yang Liu, Abhik Roychoudhury, Shanshan Liu and Jin Song Dong *International Symposium on Formal Methods (FM) 2009.*
- **[ICSE ’09]** “Footprinter: Roundtrip Engineering via Scenario and State based Models”, Ankit Goel, Bikram Sengupta and Abhik Roychoudhury, *ACM International Conference on Software Engineering (ICSE) 2009, Short paper.*
- **[TOSEM-Journal ’09]** “Interacting Process Classes”, Ankit Goel, Abhik Roychoudhury and P.S. Thiagarajan, *ACM Transactions on Software Engineering and Methodology (TOSEM), 18(4), 2009.*
- **[PASTE’08]** “Java Memory Model aware Software Validation”, Arnab De, Abhik Roychoudhury and Deepak D’Souza, *Program Analysis for Software Tools and Engineering (PASTE) 2008.*
- **[ISoLA’08]** “Debugging Statecharts via Model-Code Traceability”, Guo Liang and Abhik Roychoudhury, *IEEE International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (ISoLA), 2008.*

- [TOPLAS-Journal’08] “Dynamic Slicing on Java bytecode traces”, Tao Wang and Abhik Roychoudhury, *ACM Transactions on Programming Languages and Systems (TOPLAS)*, 30(2), 2008.
- [FMSSD-Journal’07] “Memory Model Sensitive Bytecode Verification”, Thuan Quang Huynh and Abhik Roychoudhury, *Formal Methods in System Design Journal*, 31(3), 2007.
- [ISSTA’07] “Hierarchical Dynamic Slicing”, Tao Wang and Abhik Roychoudhury, *ACM International Symposium on Software Testing and Analysis (ISSTA) 2007*. Acceptance rate = $22/101 = 21\%$.
- [ESEC-FSE’07] “Symbolic Message Sequence Charts”, Abhik Roychoudhury, Ankit Goel and Bikram Sengupta, *15th ACM SIGSOFT International Symposium on Foundations of Software Engineering (FSE), Jointly with ESEC, 2007*. Acceptance rate = $43/251 = 17\%$
- [ICSE’06] “Interacting Process Classes”, Ankit Goel, Sun Meng, Abhik Roychoudhury and P.S. Thiagarajan, *ACM/IEEE International Conference on Software Engineering (ICSE) 2006*. Acceptance rate $36/395 = 9\%$
- [ISoLA’06] “Synthesis and Traceability of Scenario-based Executable Models”, Ankit Goel and Abhik Roychoudhury, *International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (ISoLA), 2006*, IEEE Press.
- [FM’06] “A Memory Model Sensitive Checker for C#”, Thuan Quang Huynh and Abhik Roychoudhury, *International Symposium on Formal Methods (FM) 2006*. Acceptance rate $36/145 = 24.8\%$
- [CC’06] “Accurately Choosing Execution Runs for Software Fault Localization”, Liang Guo, Abhik Roychoudhury and Tao Wang, *Compiler Construction (CC) 2006*. Acceptance rate $17/72 = 23.6\%$
- [ASE’05] “Automated Path Generation for Software Fault Localization”, Tao Wang and Abhik Roychoudhury, *ACM/IEEE International Conference on Automated Software Engineering (ASE), 2005, Short Paper*.
- [ICSE’04] “Using Compressed Bytecode Traces for Slicing Java Programs”, Tao Wang and Abhik Roychoudhury, *ACM/IEEE International Conference on Software Engineering (ICSE) 2004*. Acceptance rate $58/436 = 13\%$
- [PACT’04] “Impact of Java Memory Model on Out-of-Order Multiprocessors”, Tulika Mitra, Abhik Roychoudhury and Qinghua Shen, *IEEE/ACM International Conference on Parallel Architecture and Compilation Techniques (PACT) 2004*.
- [PADL’04] “Symbolic Execution of Behavioral Requirements”, Tao Wang, Abhik Roychoudhury, Roland H.C. Yap and S.C. Choudhary, *International Symposium on Practical Applications of Declarative Languages (PADL) 2004*, Springer Verlag, LNCS 3057.
- [ACSD’03] “Communicating Transaction Processes”, Abhik Roychoudhury and P. S. Thiagarajan, *IEEE International Conference on Applications of Concurrency in System Design (ACSD) 2003*.
- [PPoPP’03] “Compactly Representing Parallel Program Executions”, Ankit Goel, Abhik Roychoudhury and Tulika Mitra, *ACM Symposium on Principles and Practice of Parallel Programming (PPoPP) 2003*.
- [ASE’03] “Depiction and Payout of Multi-threaded Program Executions”, Abhik Roychoudhury, *IEEE International Conference on Automated Software Engineering (ASE) 2003, Short paper*.

- [UNU’02] “An Executable Specification Language based on Message Sequence Charts”, Abhik Roychoudhury and P.S. Thiagarajan, *10th Anniversary Colloquium of UNU/IIST, Springer Verlag, LNCS 2757, 2002.*
- [ICFEM’02] “Formal Reasoning about Hardware and Software Memory Models”, Abhik Roychoudhury, *Intl. Conf. on Formal Engineering Methods (ICFEM) 2002, Springer Verlag, LNCS 2495.*
- [ICSE’02] “Specifying Multithreaded Java Semantics for Program Verification”, Abhik Roychoudhury and Tulika Mitra, *ACM/IEEE International Conference on Software Engineering (ICSE) 2002. Acceptance rate 45/303 = 15%*
- [CAV’01] “Automated Inductive Verification of Parameterized Protocols”, Abhik Roychoudhury and I.V. Ramakrishnan, *Computer Aided Verification (CAV) 2001, LNCS 2102, Springer Verlag.*
- [TOPLAS-Journal’04] “An Unfold/Fold Transformation Framework for Definite Logic Programs”, Abhik Roychoudhury, K. Narayan Kumar, C.R. Ramakrishnan and I.V. Ramakrishnan, *ACM Transactions on Prog. Lang. and Systems (TOPLAS), 26(3), May 2004.*
- [ASE-Journal’04] “Inductively Verifying Invariant Properties of Parameterized Systems”, Abhik Roychoudhury and I.V. Ramakrishnan, *Automated Software Engineering Journal, Kluwer Academic Publishers, 11(2), 2004.*

- **Design Tools for Embedded Systems (mostly Timing Analysis)**

- [TOPLAS] “Scratchpad Allocation for Concurrent Embedded Software”, Vivvy Suhendra, Abhik Roychoudhury and Tulika Mitra, *ACM Transactions on Programming Languages and Systems (TOPLAS), To appear.*
- [DAES-journal] “Cache-aware Optimization of BAN Applications”, Yun Liang, Lei Ju, Samarjit Chakraborty, Tulika Mitra and Abhik Roychoudhury *Design Automation for Embedded Systems, Springer, Special issue for selected papers from CODES-ISSS 2008, To appear.*
- [RTSS ’09] “Unified Cache Modeling for WCET Analysis and Layout Optimizations” Sudipta Chattopadhyay and Abhik Roychoudhury, *IEEE Real-time System Symposium (RTSS) 2009.*
- [RTSS ’09] “Timing Analysis of Concurrent Programs running on Shared Cache Multi-cores” Yan Li, Vivvy Suhendra, Yun Liang, Tulika Mitra and Abhik Roychoudhury, *IEEE Real-time System Symposium (RTSS) 2009.*
- [DAC ’09] “Generating Test Programs to Cover Pipeline Interactions”, Thanh Nga Dang, Abhik Roychoudhury, Tulika Mitra, Prabhat Mishra, *ACM Design Automation Conference (DAC), 2009. Acceptance rate = 148/682 = 21.7%*
- [DAC ’09] “Context-Sensitive Timing Analysis of Esterel Programs”, Lei Ju, Bach Khoa Huynh, Samarjit Chakraborty and Abhik Roychoudhury, *ACM Design Automation Conference (DAC) 2009, Short paper.*
- [RTS-Journal ’09] “Cache-aware Timing Analysis of Streaming Applications”, Samarjit Chakraborty, Tulika Mitra, Abhik Roychoudhury and Lothar Thiele, *Real-time Systems Journal, 41(1), 2009.*
- [CODES+ISSS’08] “Performance Debugging of Esterel Specifications”, Lei Ju, Bach Khoa Huynh, Abhik Roychoudhury and Samarjit Chakraborty, *ACM Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2008*

- [CODES+ISSS’08] “Scratchpad Allocation for Concurrent Embedded Software”, Vivy Suhendra, Abhik Roychoudhury and Tulika Mitra, *ACM Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2008*
- [CODES+ISSS’08] “Cache-aware Optimization of BAN Applications”, Yun Liang, Lei Ju, Samarjit Chakraborty, Tulika Mitra and Abhik Roychoudhury, *ACM Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2008*
- [RTAS’08] “Schedulability Analysis of MSC-based System Models”, Lei Ju, Abhik Roychoudhury and Samarjit Chakraborty, *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS) 2008*.
- [SCP-Journal’07] “Chronos: A Timing Analyzer for Embedded Software”, Xianfeng Li, Yun Liang, Tulika Mitra and Abhik Roychoudhury, *Science of Computer Programming*, Vol 69, December 2007.
- [DATE’07] “Accounting for Cache-related Preemption Delay in Dynamic Priority Schedulability Analysis”, Lei Ju, Samarjit Chakraborty and Abhik Roychoudhury, *IEEE/ACM Design Automation and Test in Europe (DATE) 2007*.
- [ASP-DAC’07] “A Retargetable Software Timing Analyzer using Architecture Description Language”, Xianfeng Li, Abhik Roychoudhury, Tulika Mitra, Prabhat Mishra and Xu Cheng, *ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) 2007*.
- [RTS-Journal’06] “Modeling Out-of-Order Processors for WCET Analysis”, Xianfeng Li, Abhik Roychoudhury and Tulika Mitra, *Real-Time Systems Journal, Springer, Vol 34, 2006*.
- [DAC’06] “Efficient Detection and Exploitation of Infeasible Paths for Software Timing Analysis”, Vivy Suhendra, Tulika Mitra, Abhik Roychoudhury and Ting Chen, *ACM Design Automation Conference (DAC) 2006. Acceptance rate 180/865 = 20.8%*
- [RTSS’05] “WCET centric data allocation to scratchpad memory”, Vivy Suhendra, Tulika Mitra, Abhik Roychoudhury and Ting Chen, *IEEE Real-Time Systems Symposium (RTSS) 2005. Acceptance rate 37/176 = 21%*
- [RTS-Journal’05] “Modeling Control Speculation for Timing Analysis”, Xianfeng Li, Tulika Mitra and Abhik Roychoudhury, *Real-Time Systems Journal, Kluwer Academic Publishers, Volume 29, 2005*.
- [ICDCIT’05] “Analyzing Loop Paths for Execution Time Estimation”, Abhik Roychoudhury, Tulika Mitra, Hemendra Singh Negi, *LNCS 3816, Springer, 2005*.
- [RTSS’04] “Modeling Out-of-Order Processors for Software Timing Analysis”, Xianfeng Li, Abhik Roychoudhury and Tulika Mitra, *IEEE Real-Time Systems Symposium (RTSS) 2004. Acceptance rate 42/187 = 22%*
- [RTSS’04] “Automatic Generation of Protocol Converters from Scenario-based Specifications”, Abhik Roychoudhury, P.S. Thiagarajan, Tuan Anh Tran and Vera A. Zvereva, *IEEE Real-Time Systems Symposium (RTSS) 2004. Acceptance rate 42/187 = 22%*
- [ICS’04] “Design Space Exploration of Caches using Compressed Traces”, Xianfeng Li, Hemendra Singh Negi, Tulika Mitra and Abhik Roychoudhury *ACM International Conference on Supercomputing (ICS) 2004. Acceptance rate 36/162 = 22%*
- [DATE’03] “Using formal techniques to Debug the AMBA System-on-Chip Bus Protocol”, Abhik Roychoudhury, Tulika Mitra and S.R. Karri, *IEEE/ACM Conference on Design Automation and Test in Europe (DATE) 2003*.

- [CODES+ISSS’03] “Accurate Estimation of Cache-related Preemption Delay”, Hemendra Singh Negi, Tulika Mitra and Abhik Roychoudhury, *ACM International Conference on Hardware Software Codesign and System Synthesis (CODES+ISSS) 2003*. Acceptance rate $30/143 = 21\%$
- [DAC’03] “Accurate Timing Analysis by Modeling Caches, Speculation and their Interaction”, Xianfeng Li, Tulika Mitra and Abhik Roychoudhury, *ACM/IEEE Design Automation Conference (DAC) 2003*. Acceptance rate $152/628 = 24\%$
- [ISSS’02] “Timing Analysis of Embedded Software for Speculative Processors”, Tulika Mitra, Abhik Roychoudhury and Xianfeng Li, *ACM International Symposium on System Synthesis (ISSS) 2002*.

• **Publications prior to Ph.D.**

- [CAV’00] “XMC : A Logic Programming based Verification Toolset”, with C.R. Ramakrishnan, I.V. Ramakrishnan, S.A. Smolka et al, *International Conference on Computer Aided Verification (CAV) 2000, LNCS vol 1855, Springer Verlag*.
- [PPDP’00] “Justifying Proofs using Memo Tables”, Abhik Roychoudhury, C.R. Ramakrishnan and I.V. Ramakrishnan, *ACM International Conference on Principles and Practice of Declarative Programming (PPDP) 2000*.
- [TACAS’00] “Verification of Parameterized Systems using Logic Program Transformations” Abhik Roychoudhury, K. Narayan Kumar, C.R. Ramakrishnan, I.V. Ramakrishnan and Scott A. Smolka, *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS) 2000, Springer Verlag, LNCS vol 1785*.
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- [PAP’97] “A rule-based data standardizer for Enterprise Databases”, Abhik Roychoudhury, I.V. Ramakrishnan and Terrence Swift, *International Conference on Practical Applications of Prolog (PAP) 1997*.
- [FST&TCS’95] “Efficient algorithms for vertex arboricity of planar graphs”, Abhik Roychoudhury and Susmita Sur Kolay, *Intl. Conf. on Foundations of Software Technology and Theoretical Computer Science (FST & TCS) 1995, Springer Verlag, LNCS 1026*.

Professional Service

- International Member of ArtistDesign Network of Excellence for Design of Embedded Systems (from January 1, 2009).
 - Program Committee Member of:
 - International Conference on Software Engineering (ICSE) 2009 - Tools Track.
 - International Symposium on Automated Technology for Verification and Analysis (ATVA) 2009.
 - International Colloquium on Theoretical Aspects of Computing (ICTAC) 2009.
 - IEEE Congress on Services 2009.
 - International Conference on Formal Engineering Methods (ICFEM) 2003, 2005, 2006.
 - International Symposium on Logic based Program Synthesis and Transformation (LOPSTR) 2004, 2005, 2007.
 - International Conference on Distributed Computing and Internet Technology (ICDCIT) 2005, 2007, 2010.
 - International Workshop on Automated Verification of Infinite-State Systems (AVIS) 2005.
 - Asian Working Conference on Verified Software (AWCVS) 2006.
 - International Workshop on Harnessing Theories for Tool Support in Software (TTSS) 2007, 2008.
 - ACM International Symposium on Applied Computing (SAC) 2006 — Track on Software Verification.
 - Co-organized International Workshop on Software Verification and Validation (SVV) 2003—06, a new workshop on software validation.
 - Guest Editor of two special issues of Electronic Notes in Theoretical Computer Science (ENTCS), where proceedings of SVV 2003, 05 were published by Elsevier.
 - Track Chair for Software Engineering in the International Conference on Distributed Computing & Internet Technology (ICDCIT) 2004, Proceedings LNCS 3347, Springer.
 - Reviewer of papers in many international journals
 - Formal Aspects of Computing Journal (FACJ), Fundamenta Informaticae (FI), Formal Methods in System Design (FMSD), International Journal on Foundations of Computer Science (IJFCS), Journal of Software and System Modeling (SoSyM), ACM Transactions on Architecture and Code Optimization (TACO), Theoretical Computer Science (TCS), ACM Transactions on Embedded Computing Systems (TECS), ACM Transactions on Programming Languages and Systems (TOPLAS), Theory and Practice of Logic Programming (TPLP), IEEE Transactions on Software Engineering (TSE)
- and conferences
- ACSD, APAQS, APSEC, ASIAN, ASP-DAC, CASES, CAV, CONCUR, CP, ECRTS, EM-Soft, FM, FoSSaCs, FST& TCS, GPCE, ICALP, ICLP, ISoLA, LCTES, PADL, PEPM, POPL, PLDI, RTSS, VMCAI.

Service to the University

- Member of *Graduate Studies Committee*, NUS School of Computing since 2003. Duties include:
 - Co-ordinator of PhD Qualifier Examination (2005-08).
 - Evaluation of PhD applications from Indian subcontinent.
 - Recruitment trips to Indian Universities, including IIT Bombay (2002) and IIT Guwahati, Jadavpur University, Bengal Engineering & Science University (2005).
 - Recruitment trip to Ho Chi Minh City, Vietnam in 2007.
- Member of *Outreach committee*, NUS School of Computing since 2009. Duties include:
 - Organization of workshop for Junior College Mathematics teachers (July 2009).
- Member of Selection Panel for Computing Alumni Assistance Award (CAAA) and Computing Student Development Fund (CSD), 2009.
- Member of Departmental Evaluation Committee (DEC) of certain academic staff for promotion (on ad-hoc basis - 2009).
- Teaching Peer-review evaluator of certain academic staff (on ad-hoc basis - 2005, 2007, 2009).
- *Assistant Professor Representative* in Executive Committee of School of Computing (2002-03).

Service to Local Community

- Research Project Evaluator for *Singapore Israel Industrial Development Foundation (SIIRD)*, Feb 2009.
- Co-organizer of Breakout Session on Computer Systems at the launch of *Advanced Digital Sciences Center (ADSC)* by University of Illinois and A*STAR at Singapore on Feb 2009.
- Member of Scientific Committee for *National Informatics Olympiad (NOI)*, Singapore (2002-2004). NOI is a creative problem solving and programming competition for High School / JC Students. Selected candidates from NOI represent Singapore in the International Olympiad in Informatics” (IOI).

Personal Data

- Married
- One son (Jishnu).
- Indian citizen.