Embedded Systems and Software Validation

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Singapore
Preface

This book attempts cover the issues in validation of embedded software and systems. There are lot of books on “embedded software and systems” as a web search with the appropriate search terms will reveal. So, why this book?

There are several ways to answer the question. The first, most direct, answer is that the current books mostly deal with the programming and/or co-design of embedded systems. Validation is often discussed almost as an after-thought. In this book, we treat validation as a first class citizen in the design process, weaving it into the design process itself.

The focus of our book is on validation, but from a embedded software and systems perspective. The methods we have covered (testing/model-checking) can also be covered from a completely general perspective, focusing only on the techniques, rather than how they fit into the system design process. But we have not done so. Even though the focus of the book is on validation methods, we clearly show how it fits into system design. As an example, we present and discuss the model checking method twice in two different ways — once at the level of system model (Chapter 2) and again at the level of system implementation (Chapter 5).

Finally, being rooted in embedded software and systems — the focus of our book is not restricted to functionality validation. We have covered at least two other aspects — debugging of performance and communication behavior. As a result, this book contains analysis methods which are rarely found in a single book — testing (informal validation), model checking (formal validation), worst-case execution time analysis (static analysis for program performance), schedulability analysis (system level performance analysis) and so on — all blended under one cover, with the goal of reliable embedded system design.

As for the chapters of the book, Chapter 1 gives a general introduction to
the issues in embedded system validation. Differences between functionality
and performance validation are discussed at a general level.

Chapter 2 discusses model-level validation. It starts with a generic dis-
cussions on system structure and behavior and zooms into behavioral mod-
eling notations such as Finite-state machines (FSMs) and Message Sequence
Charts (MSCs). Simulation, testing and formal verification of these models
are discussed. We discuss model-based testing, where test cases generated
from the model are tried out on the system implementation. We also discuss
property verification, and the well-known model checking method. The chap-
ter wraps with a nice hands-on discussion on practical validation tools such
as SPIN and SMV. Thus, this chapter corresponds to model-level debugging.

Chapter 3 discusses the issues in resolving communication incompatibil-
ities between embedded system components. We discuss different strategies
for resolving such incompatibilities, such as endowing the components with
appropriate interfaces, and/or constructing a centralized communication pro-
tocol converter. Thus, this chapter corresponds to communication debugging.

Chapter 4 discusses system level performance validation. We start with
software timing analysis, in particular Worst-case Execution Time (WCET)
analysis. This is followed by the estimation of time spent due to different
interferences in a program execution — from the external environment, or due
to other executing programs on same/different processing elements. Suitable
analysis methods to estimate the time due to such interferences are discussed.
We then discuss mechanisms to combat execution time unpredictability via
system level support. In particular, we discuss compiler controlled memories
or scratchpad memories. The chapter concludes with a discussion on time
predictability issues in emerging applications. Thus, this chapter corresponds
to performance debugging.

Chapter 5 discusses functionality debugging of embedded software. We
discuss both formal and informal approaches, with almost equal emphasis
on testing and formal verification. The first half of the chapter involves val-
idation methods built on testing or dynamic analysis. The second half of
the chapter concentrates on formal verification, in particular, software model
checking. The chapter concludes with a discussion on combining formal ver-
ification with testing. Thus, this chapter corresponds to software debugging.

Apart from some debugging/validation methods being common to Chap-
ters 2 and 5, the readers may try to read the chapters independently. A
senior undergraduate or graduate course on this topic may however read the
chapters in sequence, that is, chapters 2, 3, 4, 5.