

**NATIONAL UNIVERSITY OF SINGAPORE**

**SCHOOL OF COMPUTING**

**EXAMINATION FOR**

Semester 1: 2005/6

**CS1104 – COMPUTER ORGANISATION**

November 2005

Time allowed: 2 hours

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**INSTRUCTIONS TO CANDIDATES**

- This examination paper consists of **TEN (10)** questions and comprises **SIXTEEN (16)** printed pages. The first question contains 20 Multiple-Choice Questions (MCQs).
- Pages 14 – 16 contain three figures related to questions 7 and 8.
- This is an **OPEN BOOK** examination.
- Answer all questions. You may use a pencil to draw diagrams.
- Answer the MCQs on the MCQ Answer Sheet provided.
- Answer questions 2 – 10 on the Answer Book provided.
- For questions 7 and 8, you may, in addition, use pages 14 – 16 of this examination booklet to draw figures. Irrespective of whether you use these pages or not, please attach them to your Answer Book. Do not forget to write your matriculation number on these pages.

**Question 1 [Total 20 marks]**

This question comprises TWENTY (20) **Multiple Choice Questions**.

- Each question carries ONE (1) mark. Each question has ONLY ONE correct answer. There is no penalty for wrong answers
- Shade the correct answer on the MCQ sheet provided. Do not bend, fold or soil your MCQ Answer Sheet.

1. What are the main advantages of a single-cycle implementation of an ISA over a multi-cycle implementation?
  - A. Simpler control.
  - B. Less hardware.
  - C. Lower CPI (for a given program).
  - D. More hardware sharing.
  - E. Writing programs is less complicated.

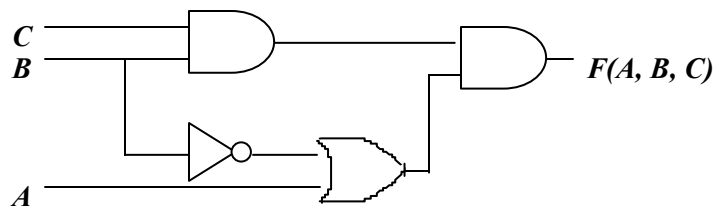
2. Which of the following relationships represents the dual of the Boolean property:

$$x + x'y = x + y$$

Choose the best answer.

- A.  $x'(x + y) = x'y'$
  - B.  $x(x'y) = xy$
  - C.  $x(1 + x') + y = xy$
  - D.  $x'(xy') = x'y'$
  - E.  $x(x' + y) = xy$
3. Simplifying the Boolean expression  $AB + A(BC)'$  yields which of the following results?
  - A. A
  - B. BC
  - C. B
  - D. AB
  - E.  $(BC)'$

4. If A, B and C are Boolean inputs to the logic circuit shown here, then what does the function  $F(A, B, C)$  compute?



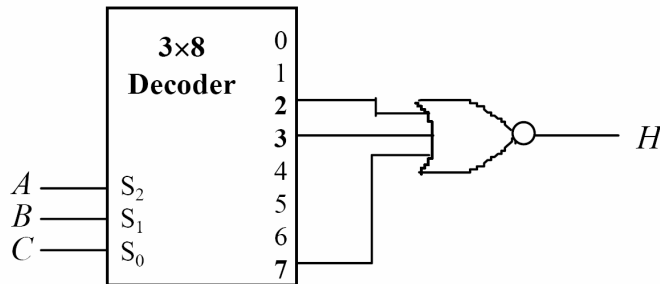
- A.  $F = A$
  - B.  $F = AB'C$
  - C.  $F = ABC$
  - D.  $F = (A+B)C$
  - E.  $F = (A+B')C$

5.  $(153)_{10}$  when converted to base 8 is equal to:
- A. 107
  - B. 132
  - C. 701
  - D. 231
  - E. 153
6. Two's complement of  $(01010)_2$  is equal to:
- A. 10101
  - B. 10011
  - C. 00101
  - D. 01100
  - E. 10110
7.  $(11011.01)_2$  when converted to base 8 is equal to:
- A. 33.2
  - B. 63.2
  - C. 63.1
  - D. 33.1
  - E. 63.01
8. 00111 is the two's complement representation of:
- A. -23
  - B. -9
  - C. -7
  - D. +22
  - E. +7
9. 10100 is the two's complement representation of:
- A. -11
  - B. +12
  - C. -12
  - D. -20
  - E. +20
10. Given a Boolean function with three variables A, B and C, the expression  $AB'C'$  is represented by:
- A.  $m_3$
  - B.  $m_4$
  - C.  $M_3$
  - D.  $M_4$
  - E.  $m_5$

11. The term  $m_{31}$  should be made up of at least \_\_\_\_\_ literals.
- A. 6
  - B. 31
  - C. 3
  - D. 4
  - E. 5
12. The correct representation of the function  $F(x,y,z) = y$  is:
- A.  $F = \sum m(0,1,4,5)$
  - B.  $F = \sum m(0,1,2,3)$
  - C.  $F = \sum m(4,5,6,7)$
  - D.  $F = \sum m(1,3,5,7)$
  - E.  $F = \sum m(2,3,6,7)$
13. If  $N$  hexadecimal digits are needed to represent the value of a number with three octal digits, what is the minimum value of  $N$ ?
- A. 1
  - B. 2
  - C. 3
  - D. 9
  - E. None of the above
14. Given two numbers  $(1234)_{m_1}$  and  $(5678)_{m_2}$ , where  $m_1$  and  $m_2$  are the bases of their number system respectively. Which of the following statement(s) can be concluded?
- A.  $m_1$  must be less than  $m_2$ .
  - B. The decimal value of  $(1234)_{m_1}$  must be less than the decimal value of  $(5678)_{m_2}$ .
  - C. The maximum value of  $m_1$  is less than the maximum value of  $m_2$ .
  - D. The minimum value of  $m_1$  is less than the minimum value of  $m_2$ .
  - E. None of the above.
15. Given two machines  $M_1$  and  $M_2$ , a program is found to execute faster in  $M_1$  than in  $M_2$ . Which of the following statement(s) is(are) true?
- A. The clock speed of  $M_1$  must be higher than that of  $M_2$ .
  - B. The average CPI of the program in  $M_1$  is lower than that in  $M_2$ .
  - C. The total number of instructions executed in  $M_1$  is smaller than that in  $M_2$ .
  - D. All (a), (b), and (c).
  - E. None of the above.
16. Given an  $N$ -bit data with  $M$ -bit address, which of the following is(are) true?
- A.  $N$  is directly proportional to  $M$  (i.e. if  $N$  is large, then  $M$  is large).
  - B.  $N$  is inversely proportional to  $M$  (i.e. if  $N$  is large, then  $M$  is small).
  - C.  $N$  must be greater than or equal to  $M$ .
  - D.  $N$  must be smaller than or equal to  $M$ .
  - E. None of the above.

17. In MIPS R2000, which data operand addressing mode takes up the largest number of instruction bits?
- Displacement addressing mode.
  - Immediate addressing mode.
  - Register addressing mode.
  - All addressing modes take up the same number of instruction bits.
  - None of the above.
18. Which of the following combinations can form a  $3 \times 8$  decoder?
- Two  $2 \times 4$  decoders and an inverter.
  - Two  $2 \times 4$  decoders and one  $1 \times 2$  decoder.
  - Four  $1 \times 2$  decoders and one  $2 \times 4$  decoder.
  - All of the above.
  - None of the above.

19. Given the following logic circuit, that uses a  $3 \times 8$  Decoder, what is  $H(A,B,C)$ ?



- $H(A,B,C) = A'.B + B.C$
  - $H(A,B,C) = A.B' + B'.C'$
  - $H(A,B,C) = B' + A.C'$
  - $H(A,B,C) = A + B'$
  - $H(A,B,C) = B'$
20. Which of the following statements is true?
- An OR function can be created from only AND gates.
  - A NOR function can be created from only NAND gates.
  - Every product-of-sums expression is a product-of-maxterms expression.
  - A minimal SOP expression can be obtained by negating all the literals and then simplifying the resulting expression.
  - None of the above.

---- End of Question 1 ----

Given below are nine main questions (Questions 2 – 10). Some of these questions are split into a number of sub-questions.

- Answers to these questions must be written in the answer-script provided.
- Answer to each main question must begin on a new page, and all its subparts must be answered in the order in which they appear in this question paper.
- Clearly indicate the question number before you start answering any question.

**Question 2 [Total 12 marks]**

Consider a 32-bit processor with 32-bit words and a byte addressable memory. Now, let us suppose that this processor has a 32-word, direct-mapped cache with 2-word cache lines.

- a. Group the 32 address bits into *tag*, *index*, and *cache-line offset* (i.e. identify the heading under which each of the 32 bits would be classified). **[3 marks]**
  
- b. Now let us consider a sequence of memory (byte) accesses made by the processor. The corresponding addresses are listed below. Copy this list in your answer-script and label each memory reference as a Hit (H) or a Miss (M). Show the final contents of the cache in a tabular form (an example of which is also shown below). In this table, fill in the TAG values and the words of the cache. Use the notation M[i] to denote the word at memory address i. Include no more than one value per word (words can be left blank). **[8 marks, -1 for each mistake]**

Memory Address (in decimal)	Hit or Miss
138	
60	
56	
140	
419	
484	
142	
392	
175	
140	
344	
487	
396	
376	
380	
160	

Index	TAG value	Word 0	Word 1
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
A			
B			
C			
D			
E			
F			

c. What is the cache hit rate for the above-mentioned memory access pattern?  
**[1 mark]**

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**Question 3 [Total 6 marks]**

A machine M is being evaluated using two programs X and Y. The instruction set of M, the CPI of each instruction, and their frequency of execution for X and Y are given below. M runs at a clock frequency of 1 GHz.

Instruction	CPI	Frequency (%)	
		Program X	Program Y
LOAD/STORE	15	20	35
Floating point ADD/SUB	12	38	25
Floating point MUL/DIV	18	12	15
Integer ADD/SUB	8	18	15
JUMP/BRANCH	6	12	10

- a. X and Y contain 10,000 and 12,000 instructions respectively. How long will X and Y require to execute on M? **[2 marks]**
- b. Now consider two possible enhancements of M: upgrading its ALU with a faster one, and upgrading its memory unit with a faster memory. The first will reduce the CPI of integer ADD/SUB instructions, and the second will reduce the CPI of LOAD/STORE instructions. The CPIs of all the other instructions will remain unchanged. Suppose that both these enhancements are simultaneously implemented in M. What is the maximum speedup that the programs X and Y can possibly experience? **[4 marks]**

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**Question 4 [Total 8 marks]**

The following MIPS assembly language program tries to sum together all the elements of an array containing 32-bit two's complement integers. The register \$a0 contains the address of the array and the register \$a1 contains the number of integers in the array.

```
doit:    lw    $t0, 0($a0)
        add  $v0, $v0, $a0
        addi $a0, $a0, 1
        addi $a1, $a1, -4
        bltz $a0, doit
```

There are multiple errors in the above program. Write down the correct version of this program and clearly indicate your corrections. **[8 marks]**

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**Question 5 [Total 12 marks]**

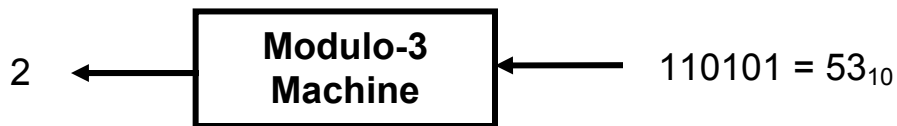
Translate the following MIPS assembly language program into a high-level language program such as C or Java. The types of all arguments should be clearly stated. Explain in one sentence what this program does. **[10 + 2 marks]**

```
easyprog:
    li $v0, 1
l1:     ble $a1, $v0, l3
        lb $t0, 0($a0)
        addi $t1, $a0, $a1
        lb $t2, -1($t1)
        beq $t0, $t2, l2
        li $v0, 0
        jr $ra
l2:     addi $a1, $a1, -2
        addi $a0, $a0, 1
        j l1
l3:     jr $ra
```

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**Question 6 [Total 12 marks]**

We want to design a finite state machine (FSM) that will take an arbitrary-sized binary integer as input, one bit at a time (starting from the most significant bit), and return the remainder after dividing this integer by 3. As an example, if the input to this machine is  $53_{10}$ , then its output is 2.



The *state* of the machine should itself represent the answer, which means that the machine will have 3 states. After the machine has read the first  $n$  bits of a number (for all  $n$ ), it should be in a state that represents the remainder obtained from dividing those  $n$  bits by 3.

Let us now assume the following notation:

$K_n$  is the  $n$ -bit number that the machine has already read.

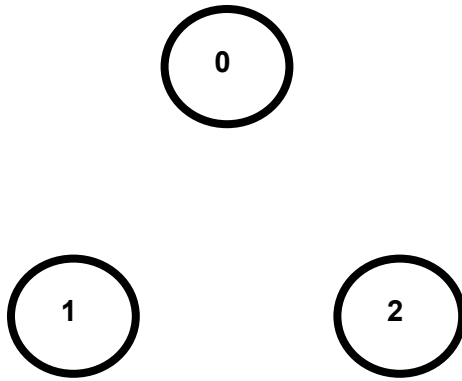
$R_n$  is the remainder obtained from dividing  $K_n$  by 3.

$Q_n$  is the quotient after  $K_n$  is divided by 3.

$X_{n+1}$  is the next bit that will be read by the machine.

We will now use the above to derive the *state transition equations* for our FSM.

- Represent  $K_n$  in terms of  $Q_n$  and  $R_n$  (i.e.  $K_n = ?$ ). **[2 marks]**
- Represent  $K_{n+1}$  in terms of  $K_n$  and  $X_{n+1}$  (i.e.  $K_{n+1} = ?$ ). **[2 marks]**
- Using the above, represent  $R_{n+1}$  in terms of  $R_n$  and  $X_{n+1}$  (i.e.  $R_{n+1} = ?$ ). This expression is the state transition equation for our FSM and  $R_{n+1}$  is our state variable that can be represented using 2 bits. **[2 marks]**
- Using the state transition equation, complete the following state transition diagram. Here, the circles represent states (i.e.  $R_n$ ) and the edges should be labeled with the input (i.e. the bit  $X_{n+1}$ ). **[2 marks]**



- e. Compute the state transition table for this FSM (one of the rows of this table has been filled for you). **[2 marks]**

Current State	Input	Next State
00	0	00
...	...	...
...	...	...

- f. Derive a ROM implementation of this state transition table. **[2 marks]**
-

**Question 7 [Total 10 marks]**

Let us assume that an ALU can perform the **max2** operation (i.e. return the largest of two inputs): `alu_result = (A_input > B_input) ? A_input : B_input;`  
The ALUOp for this instruction is MAX2.

Given this enhanced ALU, you are required to implement the **max4** instruction that writes into register `rd` the largest of four registers.

```
max4 rs, rt, rd, rm    # rd = max(rs, rt, rd, rm)
```

Note that the register `rd` serves as both, an input as well as an output register. `max4` has the following format.

Fields	op	rs	rt	rd	rm	funct
Bits	31-26	25-21	20-16	15-11	10-6	5-0

- a. The multicycle datapath that we studied in the class has been reproduced on **page 14** of this question paper. Make suitable changes to this datapath to support the `max4` instruction. You are not allowed to make changes to the main functional units themselves. You should clearly show your changes in the diagram as well as give textual explanations where necessary. Attach this diagram to your answer-script. **[5 marks]**
  
- b. The control unit that we studied in the class also needs to be changed to support the `max4` instruction. Towards this, complete the finite state machine given in **page 15** of this question paper. Attach this page to your answer-script. **[5 marks]**

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**Question 8 [Total 8 marks]**

Make suitable modifications in the single-cycle control and datapath that we studied in the class to support the `DBNZ` instruction. `DBNZ` stands for Decrement and Branch if Not Zero. It decrements the value of the `rd` register and branches if `rd` does not become equal to zero. The single-cycle datapath that we studied has been reproduced on **page 16** of this question paper for your convenience. You should clearly show your changes in this diagram as well as give textual explanations where necessary. Attach this diagram to your answer-script. Modifications to the control unit need NOT be shown. **[8 marks]**

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**Question 9 [Total 6 marks]**

A circuit to control a lock is to be designed using 10 toggle switches  $x_0, \dots, x_9$ . The lock opens only when the switches are alternately up and down. What is the specification for the corresponding switching function as a sum of minterms? **[6 marks]**

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**Question 10 [Total 6 marks]**

Simplify the following Boolean expressions. Justify each step. **[2×3 marks]**

- a.  $x' + y' + xyz'$
- b.  $a(a + b + c + \dots)$
- c.  $xz + x'y + zy$

---- End of Questions ----