NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

EXAMINATION FOR
Semester 1 AY2006/2007

CS1104 – Computer Organization

Nov/Dec 2006 **Time Allowed: 2 Hours**

INSTRUCTIONS TO CANDIDATES

1. This examination paper contains **FOUR (4)** questions and comprises **THIRTEEN (13)** printed pages, including this page. This paper totals 60 marks.

2. Answer **ALL** questions in within the space in this booklet. If you need more space, use the reverse side of the page. Indicate P.T.O if you have done so.

3. This examination may be completed in pen or pencil, and correction fluid IS allowed.

4. Only non-programmable scientific calculators are allowed. No other devices including PDAs, notebooks, mobile phones or pagers are allowed in this examination.

5. This is an Open Book examination.

6. Please write your Matriculation Number below.

MATRICULATION NO: _____

This portion is for examiner's use only

Question	Marks	Remarks
Q1	/15	
Q2	/10	
Q3	/20	
Q4	/15	
Total		

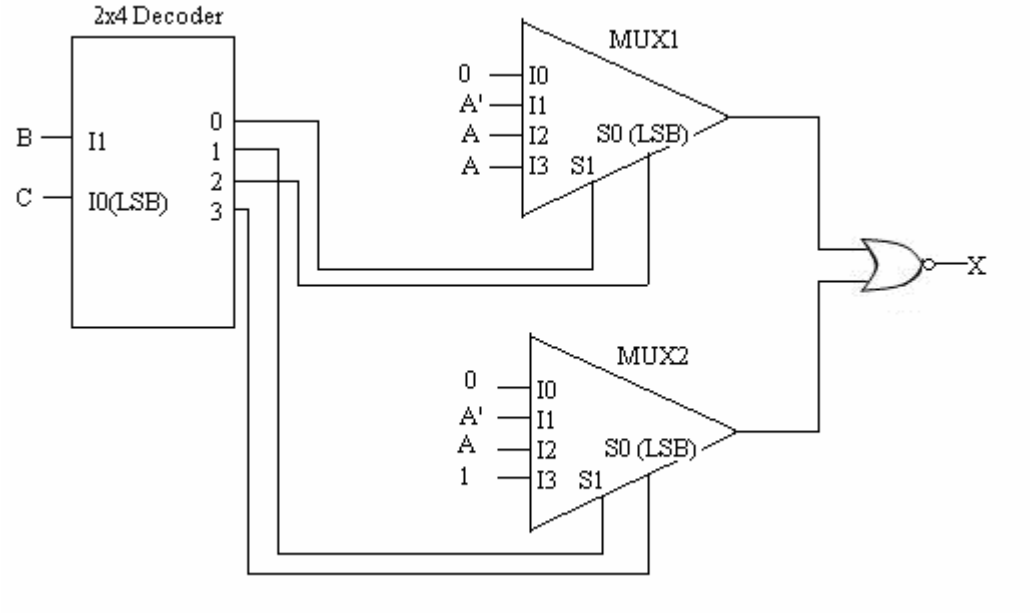
Question 1 (15 marks)

a. Using ONLY Boolean algebra (K-Maps and other methods disallowed), simplify the following functions. You may leave your answer in SOP or POS. Remember to write the theorems/axioms that you have used. (6 marks)

i) $f(A,B,C) = \sum m(0, 3, 6, 7)$

ii) $f(W,X,Y,Z) = \sum m(0, 1, 2, 4, 5, 6, 7, 8, 10, 12, 13, 14, 15)$

b. Complete the truth table given the circuit below: (6 marks)



A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

c. Using any method that you are familiar with, derive the simplified Boolean expression for X. Express your answer in Product of Sums (3 marks).

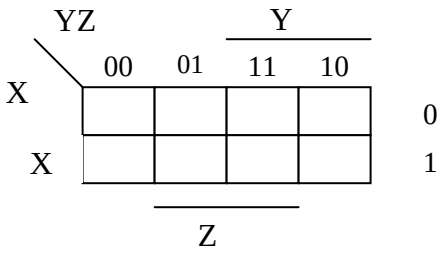
Question 2 (10 marks)

A multiply-by-3 circuit takes in a 3-bit input number N, represented by inputs X,Y,Z and produces a 4-bit number M, represented by outputs A,B,C,D, where M = 3N. Note that to fully represent M, we actually require more than 4-bits of output. Thus some ranges of M cannot be computed by our circuit. For the corresponding values of N therefore, we have a 5th output I (for Invalid), which is 1 when our circuit cannot compute the output, and 0 otherwise. In the case where I=1, we don't care about the value of M.

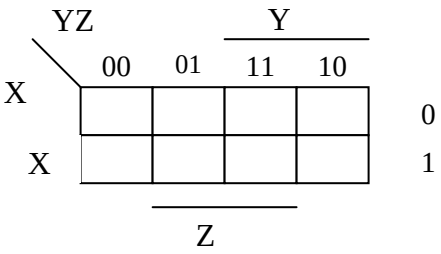
a. Derive the truth table for this circuit (3 marks).

X	Y	Z	A	B	C	D	I
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

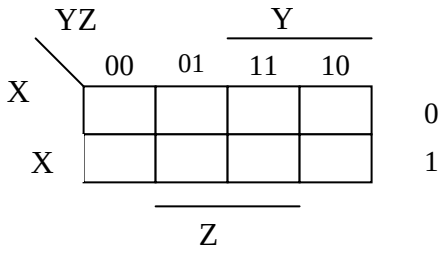
b. Using K-Maps or otherwise, derive the simplified Boolean expressions for A, B, C, D and I. (5 marks)



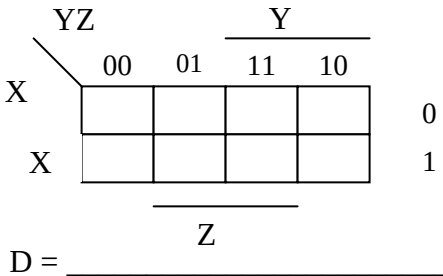
A = _____



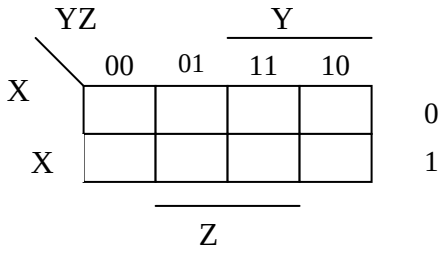
B = _____



C = _____



D = _____



I = _____

c. Sketch the circuit for output B only. (2 marks)

Question 3 (20 marks)

a. Given the recurrence relation $f_n = 2f_{n-1} + 3f_{n-2}$, where $f_0 = f_1 = 1$ and $n \geq 3$, write a fully commented MIPS assembly program that takes n in the $a0 register, and produces the first n numbers of the relation in memory location 100 onwards (i.e. f_0 in location 100, f_1 in location 101, etc) (6 marks).

b. Suppose, instead of having a 256 KB on-chip L1 cache, we have 256 KB of very fast on-chip memory that is accessed using addresses (similar to your main memory) and has the same memory access time as the cache. How similar, and how different would this scheme be from an L1 cache? You should consider your answer from the point of view of programmability, instruction set design and performance. (3 marks)

The SCPU design given in the lecture notes separates the compare instruction CMP from the branch instructions BLT, BGT and BEQ. Thus to branch if register R0 < R1, we would do:

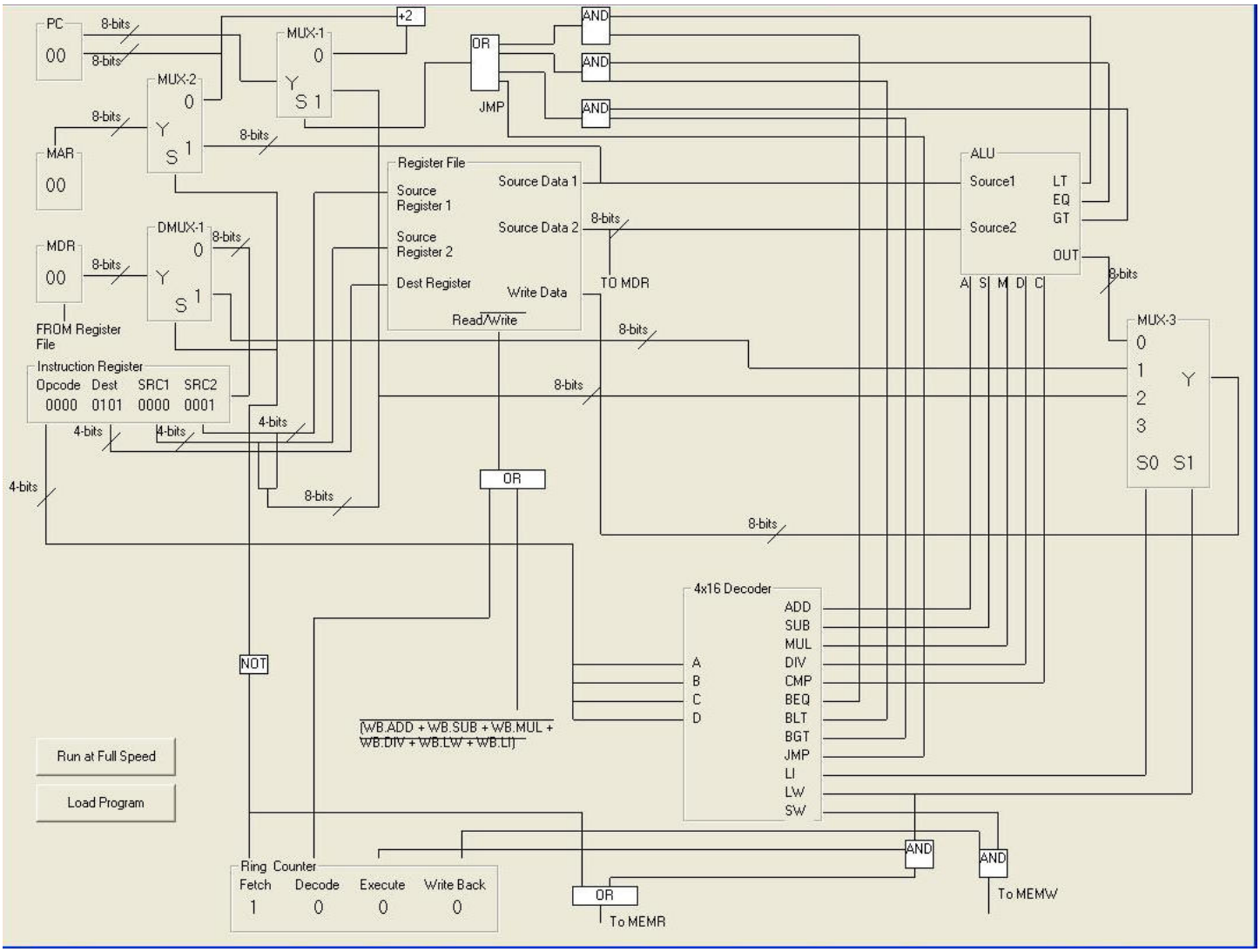
```
CMP     R0,  R1
BLT     target          ; Jump to target if R0 < R1
```

We now want to modify the BLT instruction so that it does *both* a compare AND a branch using just a single instruction:

```
BLT     R0, R1, target  ; Jump to target if R0 < R1
```

c. Design the instruction format for this new BLT instruction. You may re-use the opcode for BLT for the new version of this instruction. Note that it may not be possible to branch to the entire addressing range of the SCPU, given restrictions on the length of SCPU instructions. (3 marks)

d. For your convenience, the block diagram for the SCPU is reproduced below. Sketch the changes that you think need to be made to the diagram to accommodate the new BLT instruction. Explain briefly how your modification works, and any assumptions that you have made. (8 marks).



Question 4 (15 marks)

Given a disk drive and I/O bus with the following characteristics:

# of sides:	8
# of tracks/side:	4096
# of blocks/track:	16
# of bytes/block:	256
Disk speed:	3600 rpm

Average head seek time:	25 ms
Average head switch time:	Negligible

Bus bandwidth: 200 KBPS

a. Calculate the total capacity of the drive. (1 mark)

b. Calculate the maximum throughput of the drive. (1 mark)

c. Calculate the average amount of time it takes to read in 2048 bytes of data, assuming that the data occupy contiguous blocks (3 marks)

d. Given the following data on the memory system of a particular computer, with the virtual memory implemented using the disk system in parts a-c above, compute the average memory access time for this system. You may again assume that pages occupy contiguous blocks and that the page table is completely in main memory. (7 marks):

Cache access time:	4 ns
Cache hit rate:	98%
TLB access time:	4 ns
TLB hit rate:	90%
Main memory access time:	80 ns
Page size:	2 KB
Page fault rate:	2 %

e. Briefly explain why cache lines are usually small (between 1 word – 16 words), while VM pages are usually large (about 2-16 KB). (3 marks).