

CS1104: Computer Organisation Part I
Lab #3: A Multiply-by-6 Circuit
 (12 February 2007)

*Remember to
bring this along
to your lab!*

[This document is available on course website
http://www.comp.nus.edu.sg/~cs1104/3_ca/labs.html]

Name: _____

Matric. No: _____

Lab Group: _____

Objectives:

In this experiment, you will create a multiply-by-6 circuit using a parallel adder.

IC chips:

1. One 74LS83 chip (4-bit adder).
2. One 74LS00 chip (2-input NAND gates).

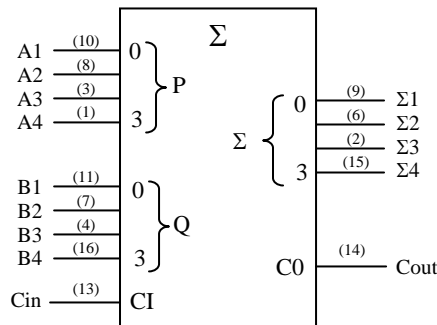


Figure 1a. Logic symbol[†] of 74LS83

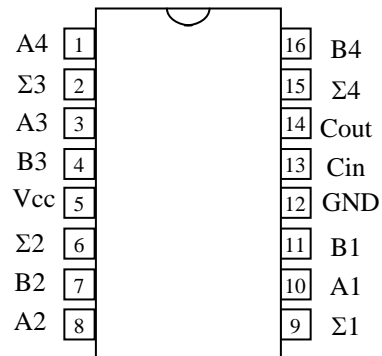


Figure 1b. Pin configuration of 74LS83

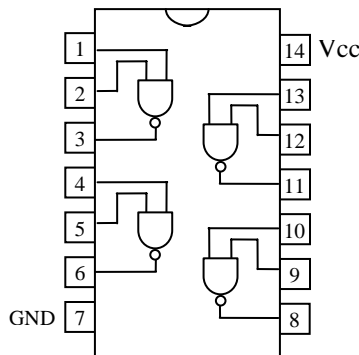


Figure 2. 74LS00

[†] This symbol is in accordance with ANSI/IEEE St 91-1984 and IEC Publication 617-12.

Procedure:

- You are to design a multiply-by-6 circuit given a 3-bit binary value ABC as its input. The circuit generates a 5-bit binary number $S_4 S_3 S_2 S_1 S_0$, and an output V .

Since the circuit may not accommodate certain input value owing to the limited number of output bits, such an input value is deemed invalid, and the corresponding output will be don't care values. The output V is used to indicate whether the input value is valid or not: 1 if the input value is valid, or 0 otherwise.

Fill in the truth table below.

Inputs			Outputs					
A	B	C	S_4	S_3	S_2	S_1	S_0	V
0	0	0	0	0	0	0	0	1
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

- Complete the K-maps for S_4 , S_3 , S_2 , S_1 and S_0 below, and write out the simplified SOP (sum-of-product) expression for each of them.

S_4

	B			
A {	0			
	C			

$S_4 =$ _____

S_3

	B			
A {	0			
	C			

$S_3 =$ _____

S_2

	B			
A {	0			
	C			

$S_2 =$ _____

S_1

	B			
A {	0			
	C			

$S_1 =$ _____

S_0

	B			
A {	0			
	C			

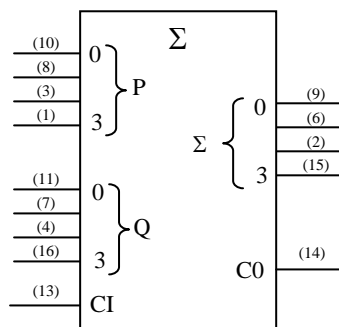
$S_0 =$ _____

3. Draw a logic circuit below to include S_4 , S_3 , S_2 , S_1 , and S_0 . You should use the least number of logic gates. Logic gates that you may use are inverters, AND gates, OR gates, XOR gates and XNOR gates. You do not need to implement this.

4. Now, implement the multiply-by-6 circuit using a 4-bit adder (74LS83 chip). The 4-bit adder is used to generate the 5-bit output $S_4S_3S_2S_1S_0$. You are not allowed to use any logic gate.

The 74LS00 chip is used to implement the output V .

Draw the logic diagram for this circuit using the block diagram of 74LS83 (given in Figure 1a) and NAND gate(s).



5. Show your circuit to your lab TA.

Marking Scheme: Report (19 marks), Circuit (6 marks); Total: 25 marks.
Your graded report will be returned to you at the next lab.