CS2100 Computer Organisation

Tutorial #4: MSI Circuits

(13 – 17 February 2012)

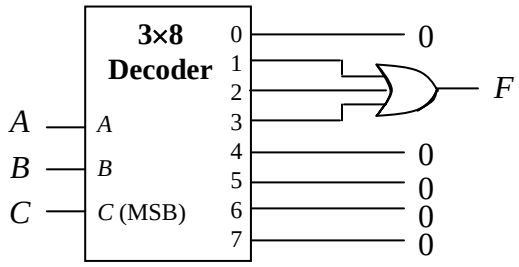
[This document is available on course website
http://www.comp.nus.edu.sg/~cs2100/3_ca/tutorials.html]

Questions 1 – 3 will not be discussed in tutorial, so please discuss them in the forum to clarify your doubts.

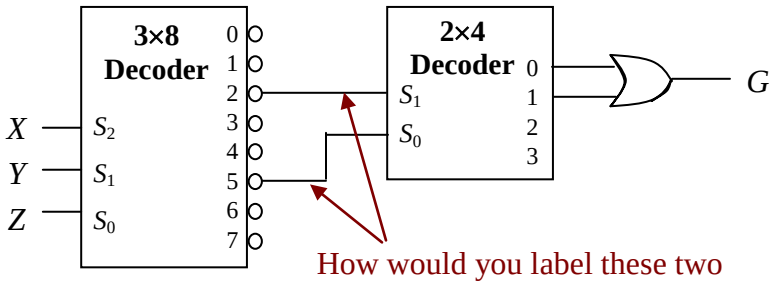
1. Given this Boolean function:

   $F(A,B,C) = \Sigma\, m(1, 2, 3)$

   We want to implement this function using a 3×8 decoder with normal outputs as shown below. Point out the mistakes in the solution below.

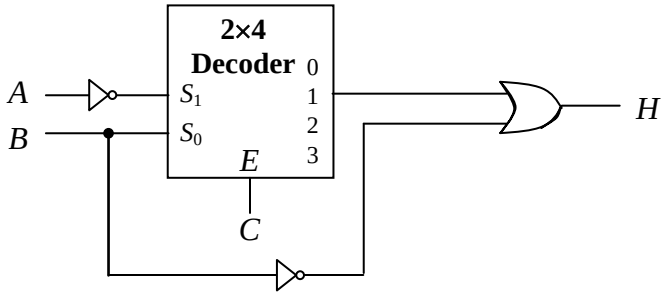


2. Given the following circuit comprising a 3×8 decoder with negated outputs and a 2×4 decoder with normal outputs, what is the Boolean function $G(X,Y,Z)$?



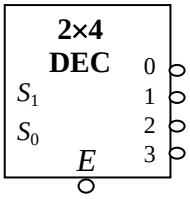
Answer: ***G(X,Y,Z)*** = _____

3. Given the following circuit comprising a 2×4 decoder with normal outputs and one-enable, what is the simplified SOP expression of Boolean function *H(A,B,C)*?



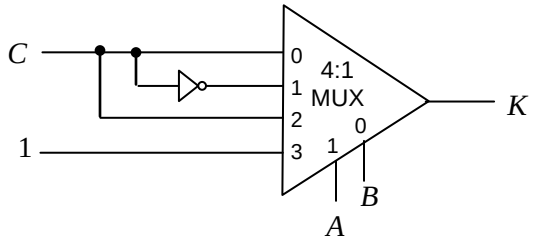
Answer: ***H(A,B,C)*** = _____

4. Given the following 2×4 decoder with negated outputs and zero-enable, how would you implement the Boolean function *J(W,X,Y,Z)* = ∏*M*(2, 3, 6, 7) without any additional logic gates?



5. Given the multiplexer below, what is Boolean function *K(A,B,C)*? Write you answer in Σ*m* notation.

   (Sometimes, for simplicity, we write the complemented variable, for example, *C'* for the second multiplexer input below, instead of drawing an inverter. Check the instruction to see if complemented literals are allowed in your solution.)



6. Realize the following functions with (i) an *8:1 multiplexer*, and (ii) a *4:1 multiplexer* using the first 2 input variables as the selector inputs. You may write complemented variables instead of drawing an inverter to derive it. If you have several choices for your answer, choose the simplest one; constant logic values 0 and 1 are simpler than literals. You may write "x" or "d" for "don't-care" (that is, its value can be either 0 or 1).

   (a) $F1(P, Q, R) = \Sigma\, m(3, 4, 6, 7)$
   (b) $F2(X, Y, Z) = \Pi\, M(1, 5, 6) \cdot D(4)$
   (c) $F3(a, b, c) = (a + b') \cdot (b' + c)$

   What if we use the last 2 input variables as the selector inputs instead?

7. Study the following circuit. Re-implement *F(a,b,c,d)* with the fewest number of 2×4 decoder with enable, and at most two logic gates.