

HUYNH PHUNG HUYNH

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CAREER OBJECTIVE

A challenging and innovative career with opportunities for professional growth

EDUCATION

- **Ph.D.** in Computer Science, National University of Singapore (Expected 2009)
Thesis: "Instruction-Set Customization for Real-Time Embedded Systems"
- **Bachelor** in Computer Science and Engineering, Ho Chi Minh University of Technology, Vietnam (2005)

RESEARCH INTERESTS

Compiler for Instruction-Set Extensible Processor, Algorithm Optimization for Hardware/Software Partitioning, Scheduling, Runtime Reconfiguration of Reconfigurable Hardware and Real-Time Embedded Systems

PUBLICATIONS

- Huynh Phung Huynh and Tulika Mitra. **Instruction-Set Customization for Real-Time Embedded Systems**. Design Automation and Test in Europe (DATE), April 2007
- Huynh Phung Huynh, Edward Sim and Tulika Mitra. **An Efficient Framework for Dynamic Reconfiguration of Instruction-Set Customization**. 7th ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2007. (**Best Paper Award Nomination**)
- Huynh Phung Huynh, Edward Sim and Tulika Mitra. **An Efficient Framework for Dynamic Reconfiguration of Instruction-Set Customization**. Springer Journal of Design Automation for Embedded Systems. (**Invited paper for special issue on best papers from CASES 2007**)
- Huynh Phung Huynh and Tulika Mitra. **Processor Customization for Wearable Bio-monitoring Platforms**. IEEE International Conference on Field Programmable Technology (FPT), December 2008
- Huynh Phung Huynh and Tulika Mitra. **Runtime Reconfiguration of Custom Instructions for Real-Time Embedded Systems**. Design Automation and Test in Europe (DATE), April 2009
- Unmesh Dutta Bordoloi, Huynh Phung Huynh, Samarjit Chakraborty and Tulika Mitra. **Evaluating Tradeoffs in Customizable Processors**. Design Automation Conference (DAC), July 2009

- **Runtime Adaptive Extensible Embedded Processors - A Survey**, Huynh Phung Huynh, Tulika Mitra. International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS), July 2009 (**Invited Paper**)

TALKS

- **An Efficient Framework for Dynamic Reconfiguration of Instruction-Set Customization** at 7th ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Salzburg, Austria, October 2007
- **Instruction-Set Customization for Real-Time Embedded Systems** at Design Automation and Test in Europe (DATE) Conference, Acropolis, Nice, France, April 2007

SKILLS AND STRENGTHS

- Good interpersonal skills and team work which are shown through the publications resulting from collaborations among my lab members and me
- Hardworking under stressful conditions as well as tight deadlines
- Passionate about excellent solutions to any research problems

HONORS AND AWARDS

- **University Silver Medal** in recognition of the outstanding academic performance among the Bachelor's graduates of the Department of IT, Ho Chi Minh City University of Technology, Vietnam, 2005
- Offered scholarship of Vietnam Ministry of Post-Telecom and Motorola Corporation, 2005
- Offered Research Scholarship at National University of Singapore, 2005-2009

TECHNICAL EXPERIENCES

- Xplorer, Stretch and ISE integrated development environment for customizable processors from Tensilica, Stretch and Xilinx respectively
- Programming languages: C, C++, C#, Java, HTML
- Operating Systems: UNIX, Window XP\ Vista

RESEARCH PROJECTS

- **Instruction-Set Customization for Real-Time Embedded Systems**
Application-specific customization of the instruction set helps simple embedded processors achieve significant performance and power efficiency. Instruction set customization extends the existing instruction set of the processor with application-specific instructions which are the most frequently executed patterns. In the context of multi-tasking embedded systems with real-time constraints, instruction set customization can reduce the worst case execution time for each constituent task so that

all the tasks can meet their deadlines. We develop a method to minimize the processor utilization of real-time multi-tasking embedded systems by instruction set customization under hardware area constraint.

After studying the efficiency of instruction set customization for the single-objective (performance), we explore the design space based on the trade-off between performance and hardware area to return multiple solutions. We develop a polynomial-time approximation algorithm to systematically evaluate the design tradeoffs.

Finally, we propose an interactive solution that enables a close feedback loop between instruction set customization and system level requirements. The key component of our solution is an efficient algorithm inspired by multi-level graph partitioning that can quickly produce high quality custom instructions for the critical region and thereby alleviate the system performance bottleneck.

➤ **An Efficient Framework for Dynamic Reconfiguration of Instruction-Set Customization**

Because the total area available for instruction set customization in a processor is quite limited, we may not be able to exploit the full potential of all the custom instructions in an application. In this context, runtime reconfiguration of the reconfigurable fabric appears promising. Here custom instructions implemented in the fabric can change over the lifetime of the application. For multi-kernel applications, runtime reconfiguration is especially attractive, as the fabric can be tailored to implement only the custom instructions required by the active kernel(s) at any point of time. We develop an efficient framework for runtime reconfiguration of application-specific custom instructions.

➤ **Processor Customization for Wearable Bio-monitoring Platforms**

Wearable bio-monitoring applications demand significant computation bandwidth from the gateway device, typically a PDA or smart phone. This is in addition to the computation bandwidth required for running regular applications on the device, such as phone calls or music players. We perform instruction set customization for wearable bio-monitoring applications to improve its computation bandwidth as well as energy consumption. This project is the practical case study for the efficiency of instruction set customization.

PERSONAL PARTICULARS

- Date of birth: 05 January 1982
- Sex: Male
- Citizenship: Vietnamese
- Marital status: Married

REFERENCES

Available upon request