Mohit **Upadhyay**

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Research Interest

Hardware Accelerators for AI-based workloads, System Design for Edge Accelerators, Computer Architecture

Education

National University of Singapore *Aug 2019 - May 2024 (Expected)*

PhD in Computer Science

Supervisor: Prof. Li-Shiuan Peh

Birla Institute of Technology and Science, Pilani *Aug 2014 - May 2019*

M.Sc.(Hons.) Physics and B.E.(Hons.) in Electrical and Electronics Engineering

Work Experience

National University of Singapore *Singapore*

Graduate Research Assistant (Mentor: Prof. Li-Shiuan Peh) *Aug 2019 - Present*

- Working on designing a dynamic NoC-based accelerator for transformer-based neural networks
- Working on designing NOVA, a NoC-style approximator for non-linear functions for attention-based neural networks on CNN accelerator (Paper presented at DATE 2024)
- Worked on designing REACT, an accelerator for transfer learning for wearables (Paper presented at DAC 2022)
- Contributed to tapeout of Shenjing, an SNN-based extremely low power inference accelerator (Paper presented at ISCAS 2023)

Xilinx Labs Asia Pacific *Singapore*

Research Intern (Mentor: Dr. Haris Javaid and Dr. Chengchen Hu) *May 2020 - July 2020*

- Worked on the design of hardware-software co-designed model of an endorsement policy evaluator in the Hyperledger Fabric blockchain distributed system on Xilinx Alveo FPGA accelerators for performance improvement (Paper presented at ICDCS 2022)

Advanced Micro Devices (AMD) India Pvt. Ltd. *Bangalore, India*

Co-op Engineer (Mentor: Dr. Prasenjit Basu and Dr. Anasua Bhowmik) *Jan 2019 - Jun 2019*

- As a part of my second undergraduate thesis, worked on HPC workload characterization by benchmarking current state-of-the-art workloads and trace models of those on simulator to study effect of vector instructions on next generation processor performance

Nanyang Technological University *Singapore*

Research Intern (Mentor: Dr. Alok Prakash and Prof. T. Srikanthan) *Jul 2018 - Dec 2018*

- As a part of my undergraduate thesis, worked on the mapping of the KLT Object Tracking Algorithm on Heterogeneous Platform on the Odroid XU-4 board using OpenCL parallel programming to improve the application performance

Technical Strengths

Programming Languages: C/C++, Shell, Verilog, System Verilog, Python, OpenCL, Pytorch
Tools & Simulators: Xilinx Vivado, Synopsys Design Compiler, Arduino

Publications

- *NOVA: NoC-based Vector Unit for Mapping Attention on a CNN Accelerator*, **Mohit Upadhyay**, Rohan Juneja, Weng-Fai Wong and Peh Li-Shiuan, **DATE 2024**
- *1.7pJ/SOP, 0.5V Scalable Neuromorphic Processor with Integrated Partial Sum Router for In-Network Computing*, B. Wang, M. M. Wong, D. Li, Y.S. Chong, J. Zhou, W. F. Wong, L. Peh, A. Mani, **M. Upadhyay**, A. Balaji, and A. T. Do, **ISCAS 2023**
- *Network-on-Chip-Centric Accelerator Architectures for Edge AI Computing*, B. Wang, K. Dong, N. Zakaria, **M. Upadhyay**, W. Wong, and L. Peh, 19th International SoC Conference, **ISOCC 2022**
- *REACT: A Heterogeneous Reconfigurable Neural Network Accelerator with Software-Configurable NoCs for Training and Inference on Wearables*, **Mohit Upadhyay**, Rohan Juneja, Wang Bo, Zhou Jun, Weng-Fai Wong, Peh Li-Shiuan, 59th Design Automation Conference, **DAC 2022**

- *Blockchain Machine: A Network-Attached Hardware Accelerator for Hyperledger Fabric*, Haris Javaid, Ji Yang, Nathania Santoso, **Mohit Upadhyay**, Sundararajarao Mohan, Chengchen Hu, Gordon Brebner, **ICDCS 2022**
- *Multi-application Based Network-on-Chip Design for Mesh-of-Tree Topology Using Global Mapping and Reconfigurable Architecture*, **Mohit Upadhyay**, Monil Shah, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, 32nd International Conference on VLSI Design, **VLSID 2019**
- *A Novel Fault-Tolerant Routing Technique for Mesh-of-Tree based Network-on-Chip Design*, **Mohit Upadhyay**, Monil Shah, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, Henning Idsøe, **IEEE TENCON 2018**
- *Fault Tolerant Routing Methodology for Mesh-of-Tree based Network-on-Chips using Local Reconfiguration*, **Mohit Upadhyay**, Monil Shah, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, International Conference on High Performance Computing and Simulation, **HPCS 2018**
- *A Novel Fault-Tolerant Routing Algorithm for Mesh-of-Tree Based Network-on-Chips*, Monil Shah, **Mohit Upadhyay**, P Veda Bhanu, J Soumya, Linga Reddy Cenkeramaddi, 22nd International Symposium on VLSI Design and Test, **VDAT 2018**

Research Projects

TVM deep learning compiler stack study for multiple hardware backends
NUS

Mentor: Dr. Jialin Li — *Aug 2020 - Dec 2020*

- Did a brief performance study of the TVM, an open deep learning compiler stack with focus on cross-compilation study for different harware backends ranging from x86 CPU, ARM based CPUs and GPUs and Xilinx FPGAs

Prefetcher Performance Study
NUS

Mentor: Dr. Trevor E. Carlson — *Jan 2020 - May 2020*

- Did a brief study of well-known prefetchers and implemented the Global history Buffer based Markov Prefetcher on the DPC simulator infrastructure and tested the implementation for performance improvement on SPEC2006 benchmarks

FPGA-based Matrix Processing Unit
NUS

Mentor: Dr. Trevor E. Carlson — *Jan 2020 - May 2020*

- Implemented a matrix processing unit on a Pynq board using HLS optimization techniques in order to accelerate performance and improve energy efficiency

Performance study of Branch Predictors
NUS

Mentor: Dr. Trevor E. Carlson — *Jan 2020 - May 2020*

- Did a study of different kinds of branch predictors and their effects on performance. Implemented the Piecewise Linear Branch Predictor on the Sniper Simulator and tested for the performance improvement on SPEC2006 benchmarks

Deep Neural Networks Inference and Training in ARM-based SoCs (Mobile GPUs)
NUS

Mentor: Dr. Bingsheng He — *Aug 2019 - Dec 2019*

- Did a study on performance of different neural network architectures on Mobile SoCs. Ported the execution of different Neural Network Architectures on the Mobile GPUs using OpenCL framework

Reconfigurable Fault Tolerant Network-on-Chips
BITS Pilani

Mentor: Dr. Soumya J. — *Aug 2017 - May 2018*

- Did a study on different router and network architectures and designed a reconfigurable network architecture with a fault tolerant routing algorithm for a Mesh-of-Tree based Network-on-Chip topology and worked on the mapping for the Mesh-of-Tree based NoC

Non-Invasive Glucometer
BITS Pilani

Mentor: Dr. Suman Kapur — *Aug 2017 - May 2018*

- Worked on the design of a glucometer which can detect the glucose level in the sample by identifying its color

UTI Detection Device
BITS Pilani

Mentor: Dr. Suman Kapur — *Aug 2017 - May 2018*

- Worked on the design of a device which can track Urine Tract Infection and the device works on the principle of detecting the infection from the color of the sample

Relevant Courses

Core Courses: Topics in Computer Science: Systems Design for Next Gen Hardware, Advanced Computer Architecture, Neural Networks and Deep Learning, Topics in Computer Science: Big Data Meets New Hardware, Computer Architecture, Embedded System Design

Other Courses: Introduction to Operating Systems, Object Oriented Programming

Teaching Experience

Fall 2023 **CG4002**: Computer Engineering Capstone Project
Fall 2022 **CS2106**: Introduction to Operating Systems

Honors & Awards

2023	**NUS Research Incentive Award**: For good academic standing and research progress in graduate studies	*NUS*
2019	**NUS Research Scholarship**: To pursue graduate studies at National University of Singapore	*NUS*
2018	**CASS Travel grant**: Travel grant to attend Computer Architecture Summer School (CASS) 2018	*IIT Kanpur*
2018	**Off-Campus Thesis Grant**: Travel grant for pursuing an off-campus thesis abroad during the final year of undergraduate studies	*BITS Pilani*

Service

MICRO 2023: Artifact Evaluation Committee Member
APCCAS 2022: Sub-reviewer
ICCAD 2021, 2022: Sub-reviewer

References

Available on Request