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## Testing and simulation

## Testing

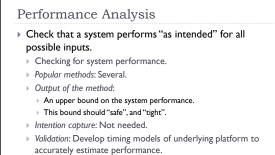
- Intention: the expected system output.
- Output of the method: Pass/Fail
- Validation: Trivial (check o/p with expected o/p)
- Key issue: Finding representative test cases.
- Simulation
  - Output: Pass/fail or estimates (for perf. simulations)
  - Validation: similar to testing
  - Key issue: Building the simulation infrastructure, apart from finding representative inputs.

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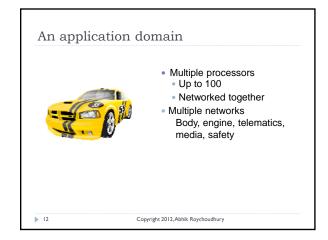
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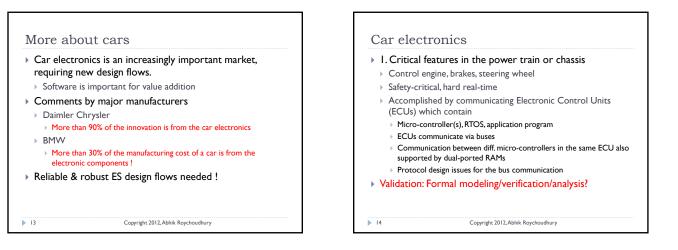
Formal Verification • Check that a system behaves "as intended" for all possible inputs. Checking for system functionality. Popular method: Model Checking Output of the method: Pass, or Counter-example evidence (if it fails). Intention captured by: Temporal Logic Properties. Validation: by automated search of the system's behavioral description. Key issue: Scalability of the search for real embedded systems. Copyright 2012, Abhik Roychoudhury

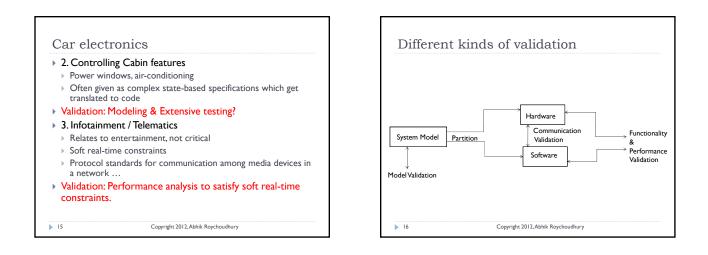


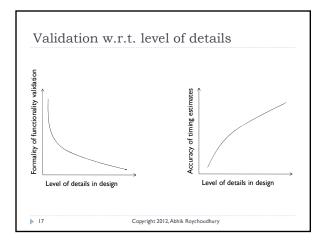
Key issue: Scalability, Growing list of new features in new platforms whose timing models need to be created.

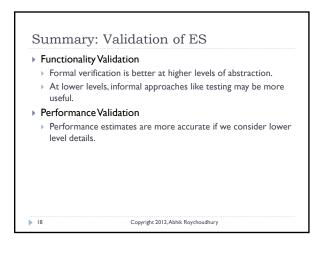
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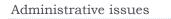








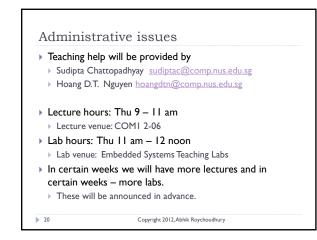




- > There will be no recording or web-cast of cs4271
- Lecturer office: COM2 #03-07
  - <u>abhik@comp.nus.edu.sg</u>
  - Consultation: anytime, preferably by e-mail appointment if possible.
  - Primarily on lecture materials.
  - Please do come in for consultation.

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<ul> <li> is as for</li> </ul>	
<ul> <li>Final 40</li> <li>Midterm</li> </ul>	-
	o assignments – 35%
	ment on Rhapsody (modeling) – 12%
	nments on SPIN/SMV (verification) – 7% + 8%
Assign	ment on Chronos (timing analysis) - 8%
<ul> <li>Assignment lesson pla</li> </ul>	nt submission dates, Midterm dates appear in IVLE n.
	nments are individual, please steer clear of plagiarism. nsions or change of dates for midterm / assignments.
Thank you	, and all the best.