Static-1 Hazard

This writeup introduces static-1 hazard in digital circuits.

A **static-1 hazard** is a temporary, unwanted glitch to logic '0' in a digital circuit's output when it is expected to remain at a steady logic '1' during an input transition. It is caused by differing propagation delays in circuit paths and is commonly found in two-level SOP circuits.

Let's begin with a simple circuit as shown in Figure 1:

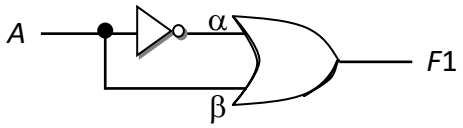


Figure 1

In this circuit, $F1 = A' + A = 1$, hence F should always be a constant 1.

However, due to the propagation delay of the inverter, when A changes from 1 to 0, the value at α (which is supposed to be A' or 1 in this case) does not change as fast as β (which is A or 0 in this case). As a result, for a very short duration both α and β are 0, resulting in $F1$ being 0! Such an incident is called a **glitch**.

The propagation delay is more pronounced in a larger circuit as shown in Figure 2 below.

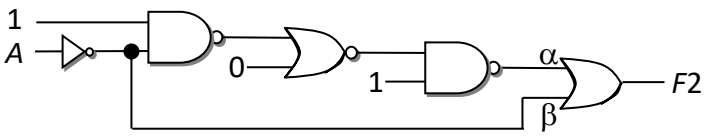
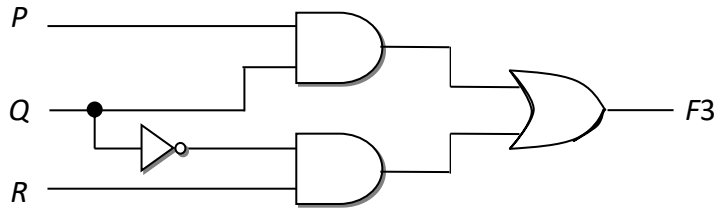


Figure 2

Here, $F2 = \alpha + \beta = A + A' = 1$. However, as α and β are on 2 paths with different propagation delays, static-1 hazard might occur. For instance, when A transits from 0 to 1, $F2$ would be 0 momentarily.

Static-1 hazards are commonly encountered in two-level AND-OR circuits. Let's look at the circuit in Figure 3:



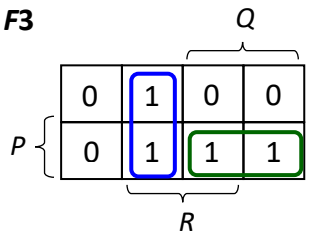


Figure 3

The circuit in Figure 3 is the implementation of the simplest SOP expression of $F3(P,Q,R) = \sum m(1,5,6,7)$ based on the K-map above, i.e. $F3 = P \cdot Q + Q' \cdot R$.

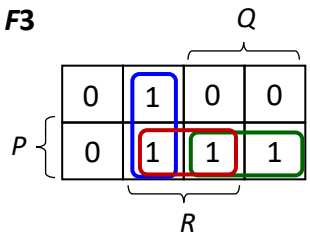
A static-1 hazard would occur when *PR*=11 and *Q* transits from 1 to 0. In other words, when the input transits from *m*7 (111) to *m*5 (101).

Removing static-1 hazard

It is known that static-1 hazards can be easily removed by introducing redundant prime implicant(s) in the circuit.

A static-1 hazard occurs when the input transits from a minterm to its neighbouring minterm in a different prime implicant. In the above example, the transition from *m*7 to *m*5 crosses from *P*·*Q* (green prime implicant) to *Q*'·*R* (blue prime implicant).

To remove the static-1 hazard, we add the prime implicant *P*·*R* (red prime implicant) that covers both *m*7 and *m*5.



The resulting SOP expression for *F*3 would then be *P*·*Q* + *Q*'·*R* + *P*·*R*.

Static-0 Hazard

Static-0 hazard is defined similarly: it is a temporary, unwanted glitch to logic '1' in a digital circuit's output when it is expected to remain at a steady logic '0' during an input transition. Explore this on your own.

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