# CS2100 Computer Organization

**AY2025/26 Semester 2**

**Assignment 2**

**(Deadline: 16 March 2026, Monday, 1pm)**

**ANSWERS**

## Instructions

1. There are **4** questions in this assignment, with a total of 40 marks.

2. This assignment is due on **Monday, 16 March 2026, 1 pm.** Late submissions will incur penalties as spelt out on Canvas > Pages: "a 10% penalty for submissions up to 3 hours late (i.e. submitting between 1.01pm and 4:00pm for a 1pm deadline), a 20% penalty for submissions up to 6 hours late, a 30% penalty for submissions up to 9 hours late, and no marks will be given for assignments submitted more than 9 hours late."

3. Enter your answers into **Canvas > Assignments > Assignment 2.** You are allowed 3 attempts. Only your last submission (not your best) will be graded. You are not to request us to ignore your last submission (including a late submission), nor can you choose the version you want us to grade.

4. Please read and follow the instructions on how to format your answers. This is important as your answers will be auto-graded, so any answer that departs from the specified format will be graded as incorrect.

5. You could refer to the document **assign2_25s2_qns.pdf** at **Canvas > Files > Assignments > Assignment 2** in which all the questions are presented in a single file for your convenience.

6. For questions 2(b) and 2(d), you must use the 5-variable K-map template found at **Canvas > Files > Assignments > Assignment 2** (available in .docx and .pdf formats). Complete your work on the template and upload your images as separate **PNG** or **JPG** files directly into the corresponding Canvas Quiz questions. Ensure your images are clear and legible, as unreadable images cannot be graded; avoid using the HEIC format if you are submitting via mobile phone.

7. Do not use special fonts (eg: Chinese, Vietnamese, etc.) as the quotation marks may not be recognised by Canvas.

8. You should do these assignments on your own. Do not discuss the assignment with others.

9. Please post on QnA "Assignments" topic if you have any queries on this assignment.

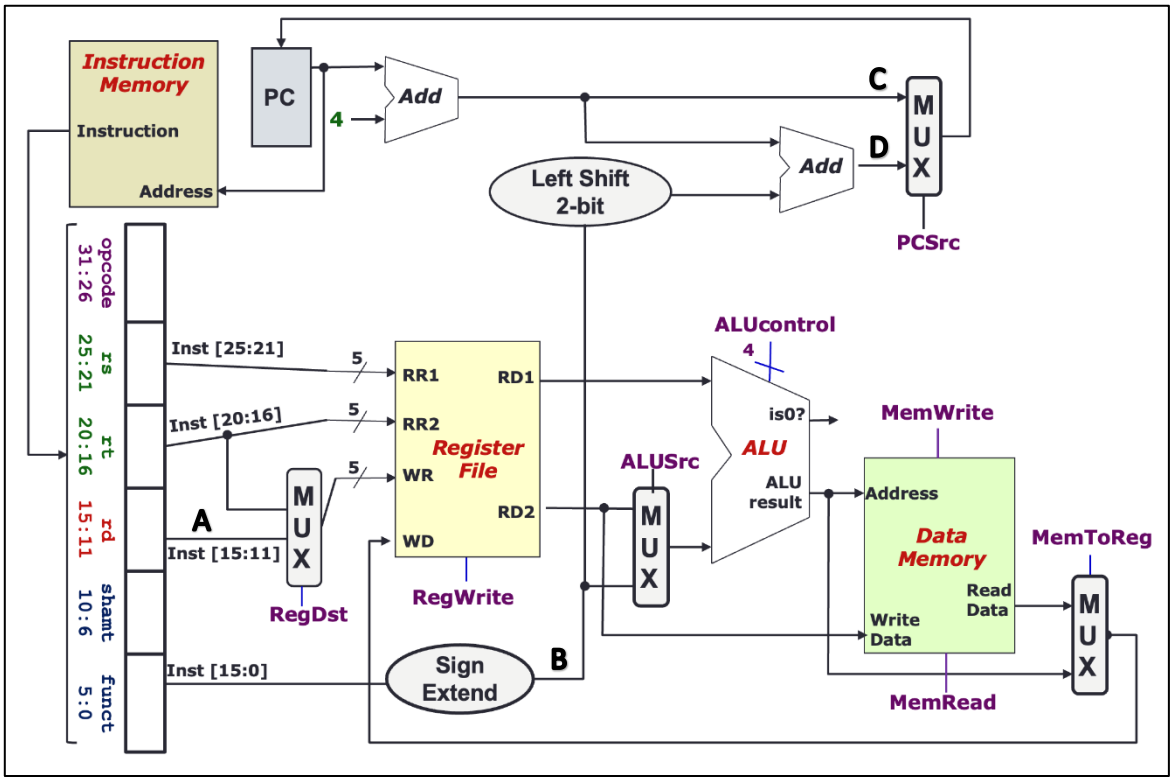
**Part I: MIPS Datapath** (20 marks)

**Question 1.** (20 marks)

Consider the MIPS Datapath with the initial values of the registers and memory as shown below. Values preceded by 0x are in hexadecimal.

| MIPS Registers | | | |
|---|---|---|---|
| R0 (r0) = 0x00000000 | R1 (at) = 0x00002000 |
| R2 (v0) = 0x00000001 | R3 (v1) = 0x0000000A |
| R4 (a0) = 0x00000005 | R5 (a1) = 0x7FFFF000 |
| R6 (a2) = 0x7FFFF004 | R7 (a3) = 0x000000B0 |
| R8 (t0) = 0x00000001 | R9 (t1) = 0x00000C00 |
| R10 (t2) = 0x0000C000 | R11 (t3) = 0xFFFFFFF0 |
| R12 (t4) = 0xF0000000 | R13 (t5) = 0x00000FFF |
| R14 (t6) = 0x00006200 | R15 (t7) = 0x00000E00 |
| R16 (s0) = 0x00300000 | R17 (s1) = 0x00000C00 |
| R18 (s2) = 0x00040200 | R19 (s3) = 0x00011000 |
| R20 (s4) = 0x00030200 | R21 (s5) = 0x00000000 |
| R22 (s6) = 0x00055000 | R23 (s7) = 0xF0000000 |
| R24 (t8) = 0x00000005 | R25 (t9) = 0x0000D000 |
| R26 (k0) = 0x00000000 | R27 (k1) = 0x00000000 |
| R28 (gp) = 0x10008000 | R29 (sp) = 0x7FFFEFF4 |
| R30 (s8) = 0x1000000F | R31 (ra) = 0x00400018 |

| Memory Address | Data |
|---|---|
| 0xFFFFFF94 | 200 |
| 0xFFFFFF98 | 300 |
| 0xFFFFFF9C | 400 |
| 0xFFFFFFA0 | 500 |
| 0xFFFFFFA4 | 600 |



**Question 1**. (continue…)
The current PC value and the address of the first instruction is 0x**00002000. T**he following instructions are being executed:

```
        I1: addi $t0, $zero, 0
        I2: addi $t1, $zero, 0
        I3: addi $t4, $t3, -88
loop:
        I4: lw   $t2, -4($t4)
        I5: add  $t1, $t1, $t2
        I6: addi $t4, $t4, 4
        I7: addi $t0, $t0, 1
        I8: bne  $t0, $a0, loop
```

Fill in the values of the fields in the table below:

- Column 2 should contain the values **after executing instruction I4 in the first iteration** of the loop.
- Column 3 should contain the values **after executing instruction I8 in the second iteration** of the loop.

For rows marked with *, your answers must follow the base given (0b for binary, 0x for hexadecimal), and you must write all the required digits with A to F in capital letters, or it will be graded as wrong even if the value is correct. You do NOT need to include the prefix 0b or 0x in your answers. For rows without *, the answers are to be in decimal, and you are NOT to include leading zeroes in your decimal answers. If a control signal is a don't-care value, enter X.

| Fields | Values for Instruction I4 | Values for Instruction I8 |
|---|---|---|
| RegDst | **0** | **0 or X** |
| MemRead | **1** | **0** |
| MemWrite | **0** | **0** |
| ALUcontrol* | **0b 0010** | **0b 0110** |
| RegWrite | **1** | **0** |
| Instruction[31-26]* | **0b 100011** | **0b 000101** |
| Instruction[25-21]* | **0b 01100** | **0b 01000** |
| Instruction[20-16]* | **0b 01010** | **0b 00100** |
| Instruction[15-0]* | **0x FFFC** | **0x FFFB** |
| A* | **0x 1F** | **0x 1F** |
| B* | **0x FFFFFFFC** | **0x FFFFFFFB** |
| RD1* | **0x FFFFFF98** | **0x 00000002** |
| RD2* | **0x 0000C000** | **0x 00000005** |
| ALU Result* | **0x FFFFFF94** | **0x FFFFFFFD** |
| ALUSrc | **1** | **0** |
| RR1 | **12** | **8** |
| RR2 | **10** | **4** |
| MemToReg | **1** | **0 or X** |
| C* | **0x 00002010** | **0x 00002020** |
| D* | **0x 00002000** | **0x 0000200C** |

**Answers:** The instructions are decoded as below for your reference. Students are not expected to provide this solution or working. They just need to fill the values in the table below.

**lw $t2, -4($t4)** is decoded as:
opcode rs rt immediate
100011 01100 01010 1111111111111100
-4 in 2s complement, 16 bit representation = 1111111111111100 = 0xFFFC

**bne $t0, $a0, loop** (loop = -5) is decoded as:
opcode rs rt immediate
000101 01000 00100 1111111111111011
-5 in 2s complement, 16 bit representation = 1111111111111011 = 0xFFFB

**Marking scheme:** Each answer in the above table carries 0.5 mark. Most of these answers should be auto graded by Canvas and they should follow the answer format.

**Part II. Boolean algebra, logic circuits and simplification** (20 marks)

Note that in general, unless otherwise stated, complemented literals are not available. Constants 0 and 1 are always available, and they are considered (degenerated form of) SOP and POS expressions.

Remember to write · for the AND operation, or mark will be deducted. If you are typing your answers, you may use the full stop (.) for AND and the single quote (′) for complement. Do not use other alternative symbols (such as $\sim A$, $\neg A$, $\bar{A}$, etc. for the complement of $A$, write $A'$ instead).

Unless otherwise stated, workings are not required.

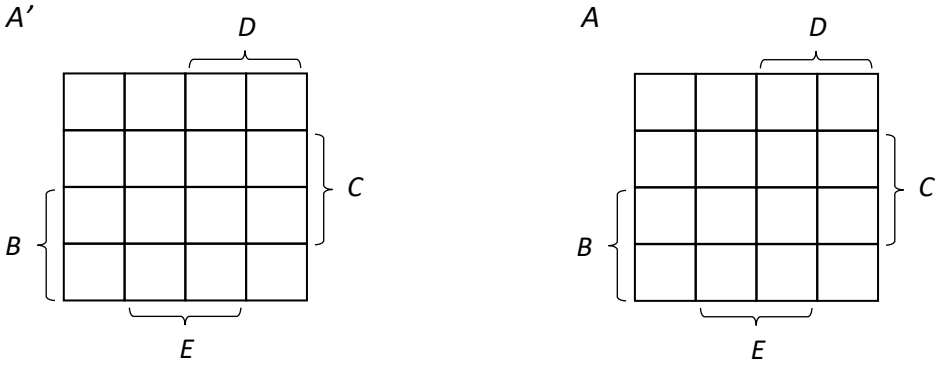
The above instructions apply for subsequent assignment, midterm test and the final exam.

Note that no partial credits will be awarded for incorrect answers for most of the questions.

Please follow these instructions which are to expedite auto-grading. If your answers depart from the stipulated format, they will be regarded as incorrect.

- Do not omit the dot operator for AND.
- Do not include unnecessary parentheses. For example, if the answer is *B*+*A*·*C*′, do not write *B*+(*A*·*C*′) or (*B*+*A*·*C*′) or (*B*)+(*A*·*C*′).
- Do not add spaces in your expression. For example, if the answer is *B*+*A*·*C*′, do not write *B* + *A*·*C*′ or *B*+*A* · *C*′ or *B* + *A* · *C*′.
- In writing a product term or a sum term, put the literals in alphabetical order, for example, write *A*′·*B*′·*C* instead of *A*′·*C*·*B*′, *B*′·*A*′·*C*, *B*′·*C*·*A*′, *C*·*A*′·*B*′ or *C*·*B*′·*A*′. Do the same for sum terms.
- In writing an SOP expression, write all product terms that correspond to the essential PIs before the product terms that correspond to the non-essential PIs. Among the EPIs, order them by their length in increasing order. Similarly, among the non-essential PIs, order them by their length in increasing order. For example, if *Y*·*Z* is an EPI and *X* is not, then write *Y*·*Z*+*X* instead of *X*+*Y*·*Z*; if *X* and *Y*·*Z* are both EPIs (or both non-essential PIs), then write *X*+*Y*·*Z* instead of *Y*·*Z*+*X*. Product terms of the same essentiality and length may be in any order. For example, if *P*·*Q* and *P*′·*R* are both essential (or both non-essential), then *P*·*Q*+*P*′·*R* and *P*′·*R*+ *P*·*Q* are both acceptable.

**Question 2** (Total: 5 marks)
You are to follow the layout of the 5-variable (*A,B,C,D,E*) K-map below for parts (b) and (d).




(a) A prime implicant in a 5-variable K-map contains 4 minterms. How many literals are there in the product term associated with that prime implicant? Write a single integer in your answer. (1 mark)

(b) Given $F(A,B,C,D,E) = \Sigma m(1,3,7,8,9,11,15,16,17,19,23,24,25,27,31)$, fill in the K-map for $F$. You are to upload an image. (1 mark)

(c) What is the simplified SOP expression for $F$? (You do not need to write $F =$) (1 mark)

(d) Given $G(A,B,C,D,E) = F(A,B,C,D,E) + \Sigma x(0,2,10,18,26,30)$, where $x$'s are the don't cares, fill in the K-map for $G$. You are to upload an image. (1 mark)

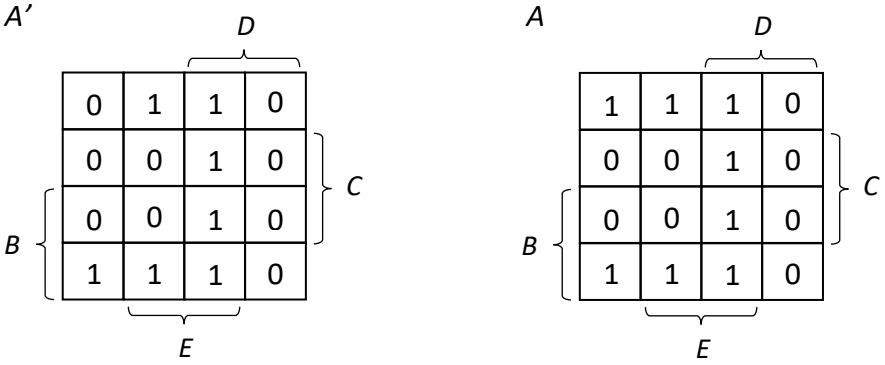
(e) What is the simplified SOP expression for $G$? (You do not need to write $G =$) (1 mark)

**Answers**

(a) **3** literals

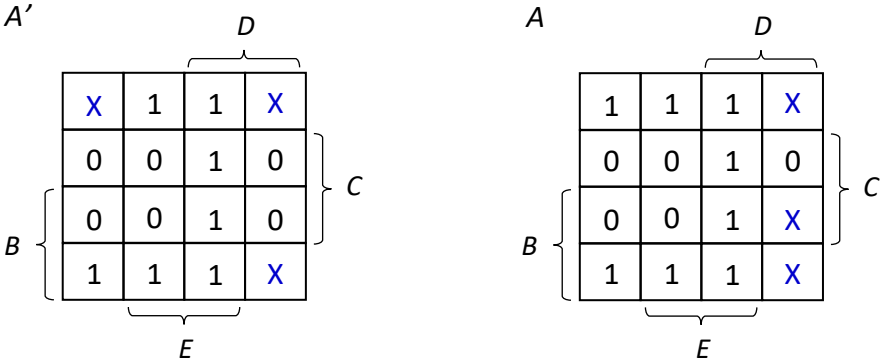
Tutors: Need to grade (b) and (d) manually.

(b)




(c) $D \cdot E + C' \cdot E + A \cdot C' \cdot D' + B \cdot C' \cdot D'$ (Also accept: $C' \cdot E + D \cdot E + A \cdot C' \cdot D' + B \cdot C' \cdot D'$, or $D \cdot E + C' \cdot E + B \cdot C' \cdot D' + A \cdot C' \cdot D'$, or $C' \cdot E + D \cdot E + B \cdot C' \cdot D' + A \cdot C' \cdot D'$)

(d)




(e) $C' + D \cdot E$

**Question 3** (Total: 5 marks)

The 8,4,-2,-1 code and 2421 code for the ten decimal digits 0 to 9 are shown in the table below:

| Decimal digit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|---|
| 8,4,-2,-1 code | 0000 | 0111 | 0110 | 0101 | 0100 | 1011 | 1010 | 1001 | 1000 | 1111 |
| 2421 code | 0000 | 0001 | 0010 | 0011 | 0100 | 1011 | 1100 | 1101 | 1110 | 1111 |

(Note that there are only ten decimal digits, hence there are 6 invalid codes for each coding scheme.)

You are to design a circuit that takes in a 4-bit 8,4,-2,-1 code *ABCD* and generates its equivalent 4-bit 2421 code *PQRS*. For example, if the input is 0101 (digit 3 in 8,4,-2,-1 code), then the output is 0011 (digit 3 in 2421 code).

(a) Write the simplified SOP expression for $P$. (You do not need to write $P =$) (1 mark)

(b) Write the simplified SOP expression for $S$. (You do not need to write $S =$) (1 mark)

(c) One simplified SOP expression for $R$ is *A·C'·D'+A·C·D+A'·C·D'+A'·C'·D* – this is given to help you get the correct answer for part (d). (Note that there is more than one simplified SOP expression for $R$.)

This simplified SOP expression for $R$ is implemented using a two-level AND-OR circuit. There are no limits on the fan-in of the AND and OR logic gates. Assuming that the propagation delay of a logic gate with fan-in of *n* is 5*n* pico-seconds, what is the minimum propagation delay, in pico-seconds, of the two-level AND-OR circuit that implements the simplified expression for $R$ given above? Write your answer as a single integer. (1 mark)

(d) Write the simplified SOP expression for $Q$. (You do not need to write $Q =$) (2 marks)

**Answers**

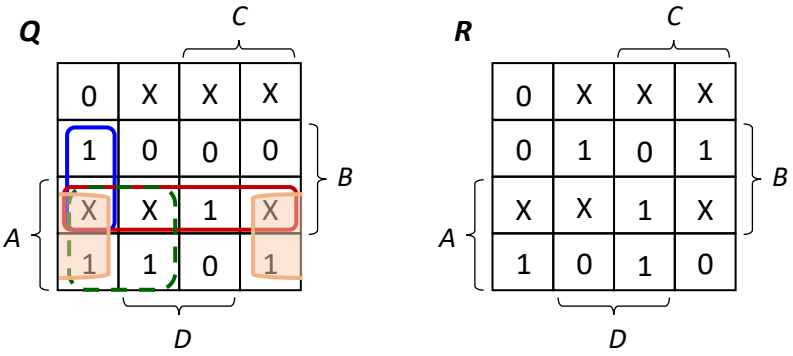
(a) ***A*** (b) ***D***

(c) (1+3+4)×5ns = **40**ns.
(Inverter: 5ns; 3-input AND gates: 3x5ns; 4-input OR gate: 4x5ns).

(d) ***A·B+B·C'·D'+A·C'+A·D'*** or ***A·B+B·C'·D'+A·D'+A·C'***

(Note that *A·B* and *B·C'·D'* are EPIs, so they must appear before the other two product terms, and *A·B* must appear before *B·C'·D'*.)

| 8,4,-2,-1 code | | | | 2421 code | | | |
|---|---|---|---|---|---|---|---|
| ***A*** | ***B*** | ***C*** | ***D*** | ***P*** | ***Q*** | ***R*** | ***S*** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | X | X | X | X |
| 0 | 0 | 1 | 0 | X | X | X | X |
| 0 | 0 | 1 | 1 | X | X | X | X |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | X | X | X | X |
| 1 | 1 | 0 | 1 | X | X | X | X |
| 1 | 1 | 1 | 0 | X | X | X | X |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |




Marking Scheme: If the expression is correct but the positions of the EPIs *A·B* and *B·C'·D'* are wrong:

- *B·C'·D'+A·B+…*.: Both EPIs in front but in the wrong order – award 1 mark.
- *A·B* in front but *B·C'·D'* not at the second position – award 1 mark.
- Other cases: no mark.

**Question 4** (Total: 10 marks)

Refer to the writeup "Static-1 Hazards" on Canvas > Files > Assignments > Assignment 2 for an introduction to static-1 hazards.

Given a 4-variable Boolean function $H(A,B,C,D) = \Sigma m(4,6,7,10,11,14,15) + \Sigma x(0,5,8)$ where $x$'s are don't-cares, answer the following parts.

(a) How many prime implicants are there in the K-map of $H$? (1 mark)

(b) How many essential prime implicants are there in the K-map of $H$? (1 mark)

(c) What is the simplified SOP expression for $H$? (You do not need to write $H =$) (2 marks)

(d) What is the simplified POS expression for $H$? (You do not need to write $H =$) (2 marks)

(e) The simplified SOP expression for $H$ has a static-1 hazard when the circuit transits from a certain minterm *m*X to another minterm *m*Y. Write the answer as **X,Y** (i.e. X followed by a comma followed by Y, with no space between them). For example, if there exists a static-1 hazard from *m*12 to *m*7, you are to write "12,7" (without the quotation marks). There could be more than 1 transition that causes a static-1 hazard; you need only provide one. (2 marks)

(f) What is the product term you need to add to the SOP expression for $H$ to eliminate all static-1 hazards? That is, suppose your answer for part (c) is $H = \Phi$ and the SOP expression for $H$ to eliminate all static-1 hazards is $H = \Phi + \Psi$, then you are to write the product term $\Psi$. (2 marks)

**Answers**

(a) **5** PIs: *A*·*C*, *A*'·*B*, *B*·*C*, *A*'·*C*'·*D*' and *A*·*B*'·*D*'.
(Note that *B*'·*C*'·*D*' is not a prime implicant.)

(b) **1** EPI: *A*·*C*.

(c) $A \cdot C + A' \cdot B$ (Marking scheme: Award 1 mark for $A' \cdot B + A \cdot C$.)

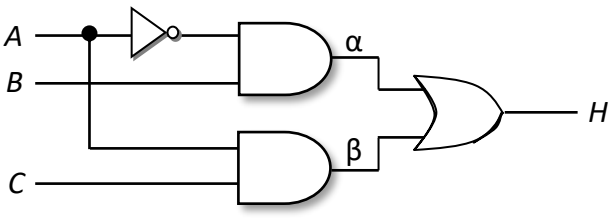
(d) $(A + B) \cdot (A' + C)$ or $(A' + C) \cdot (A + B)$

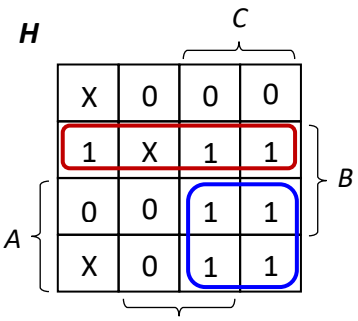
Working: $H' = A' \cdot B' + A \cdot C'$ or $A \cdot C' + A' \cdot B'$

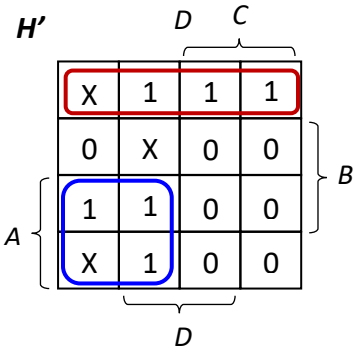
(e) Any of the two answers: **14,6** or **15,7**
A static-1 hazard occurs when the circuit transits from a minterm to its neighbouring minterm crossing into another prime implicant of its SOP expression. The two possible transitions are from *m*14 (1110) to *m*6 (0110), or from *m*15 (1111) to *m*7 (0111), i.e. *A* transits from 1 to 0 when *BC* = 11.

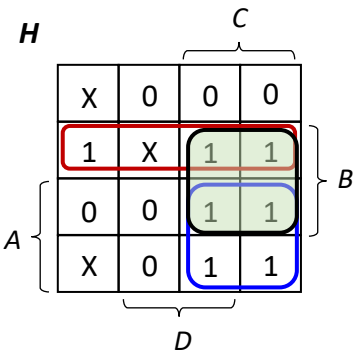
Marking scheme: Award 1 mark for **6,14** or **7,15**.

(f) $H = A \cdot C + A' \cdot B + \boldsymbol{B \cdot C}$
The answer is $\boldsymbol{B \cdot C}$, which covers the transitions (*m*14 to *m*6, and *m*15 to *m*7).

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