CS2100 Computer Organization

AY2025/26 Semester 2

Assignment 3

(Deadline: 6 April 2026, Monday, 1pm)

ANSWERS

Instructions

1. There are **5** questions in this assignment, with a total of 20 marks.

2. This assignment is due on **Monday, 6 April 2026, 1 pm.** Late submissions will incur penalties as spelt out on Canvas > Pages: "a 10% penalty for submissions up to 3 hours late (i.e. submitting between 1.01pm and 4:00pm for a 1pm deadline), a 20% penalty for submissions up to 6 hours late, a 30% penalty for submissions up to 9 hours late, and no marks will be given for assignments submitted more than 9 hours late."

3. Enter your answers into **Canvas > Assignments > Assignment 3.** You are allowed 3 attempts. Only your last submission (not your best) will be graded. You are not to request us to ignore your last submission (including a late submission), nor can you choose the version you want us to grade.

4. You could refer to the document **assign3_25s2_qns.pdf** at **Canvas > Files > Assignments > Assignment 3** in which all the questions are presented in a single file for your convenience.

5. Please read and follow the instructions on how to format your answers. This is important as your answers will be auto-graded, so any answer that departs from the specified format will be graded as incorrect.

6. Do not use special fonts (eg: Chinese, Vietnamese, etc.) as the quotation marks may not be recognised by Canvas.

7. You should do these assignments on your own. Do not discuss the assignment with others.

8. Please post on QnA "Assignments" topic if you have any queries on this assignment.

To tutors: All autograded except for

- Q2(c): Need to check the name of the circuit (students may use different words)
- Q3(b) and (c): Need to check that the magnitude comparator returns 1 if and only if $P=R$.

Note that in general, unless otherwise stated, complemented literals are not available. Constants 0 and 1 are always available, and they are considered (degenerated form of) SOP and POS expressions.

Remember to write · for the AND operation, or mark will be deducted. If you are typing your answers, you may use the full stop (.) for AND and the single quote (′) for complement. Do not use other alternative symbols (such as $\sim A$, $\neg A$, $\bar{A}$, etc. for the complement of A, write A' instead).

Unless otherwise stated, workings are not required.

The above instructions apply for subsequent assignment, midterm test and the final exam.

Important Instructions (don't skip this!):

When listing out the minterms/maxterms, you are to write them in increasing order separated by comma, with no parentheses, space and other punctuation. For example, if the answer is $\boldsymbol{\Sigma m(1,2,3,5)}$, enter **1,2,3,5**. Answers such as (1,2,3,5) (with parentheses), 1, 2, 3, 5 (with additional spaces), 1,5,2,3 (not in increasing order), and 1,2,3,3,5 (duplicate numbers) will all be graded as wrong with no partial credit given. Pay attention to the order of the variables in the given function.

When typing the simplified SOP expressions, use . for AND, + for OR, and ' for complement. Do not add spaces, and do not add unnecessary parentheses.

Question 1. (Total: 3 marks)

Figure 1 below shows a logic circuit with a 4-bit parallel adder and a half adder. The half adder has the outputs C (carry) and S (sum). This circuit takes in two 4-bit unsigned integers A ($A=A_3A_2A_1A_0$) and B ($B=B_3B_2B_1B_0$) and generates the value $A + 2B$ in the 6-bit output F ($F= F_5F_4F_3F_2F_1F_0$).

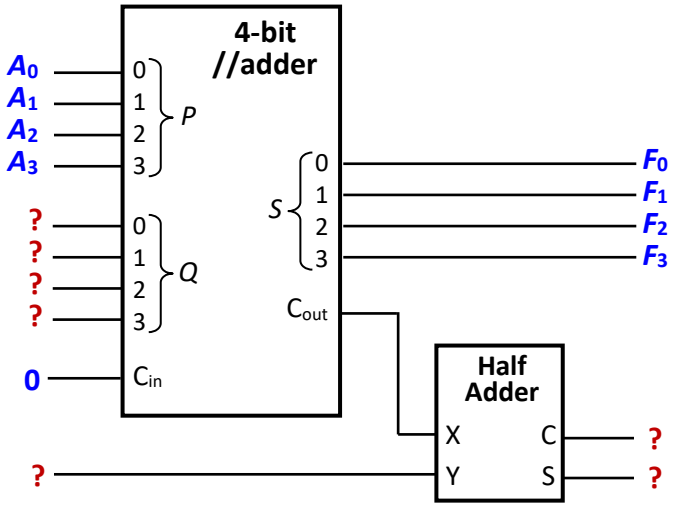


Figure 1

(a) What is connected to the input Q_3 of the 4-bit parallel adder? (0.5 mark)

(b) What is connected to the input Q_2 of the 4-bit parallel adder? (0.5 mark)

(c) What is connected to the input Q_1 of the 4-bit parallel adder? (0.5 mark)

(d) What is connected to the input Y of the half adder? (0.5 mark)

(e) What is the output C of the half adder? (0.5 mark)

(f) What is the output S of the half adder? (0.5 mark)

Answers:

(a) B_2 (b) B_1 (c) B_0 (d) B_3 (e) F_5 (f) F_4

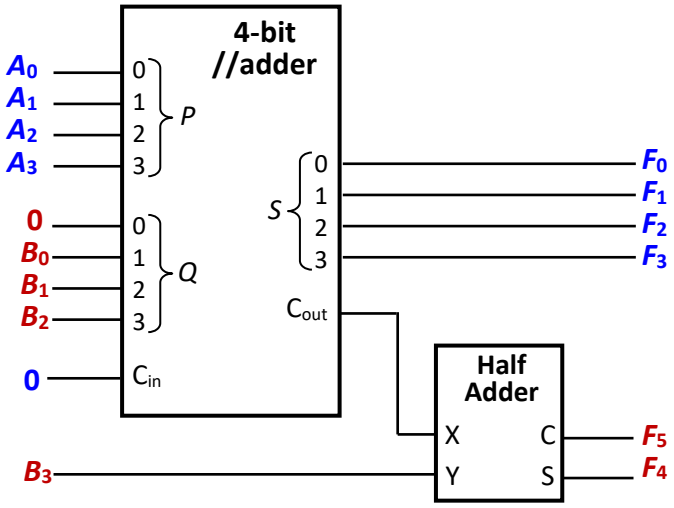

4-bit
//adder
A0
A1
A2
A3
0
1
2
3
P
0
B0
B1
B2
0
1
2
3
Q
0
Cin
S
0
1
2
3
F0
F1
F2
F3
Cout
Half
Adder
X
Y
C
S
F5
F4
B3

Figure 1

Question 2. (Total: 3 marks)

Figure 2 below shows a function *F2*(*P*,*Q*,*R*) implemented using a 3×8 decoder with one-enable and active-high outputs and an 8:1 multiplexer. Note that *A* is the MSB input and *C* the LSB input for the decoder, and S_2 is the MSB selector and S_0 the LSB selector for the multiplexer (following the standard notation where the largest subscript is the MSB).

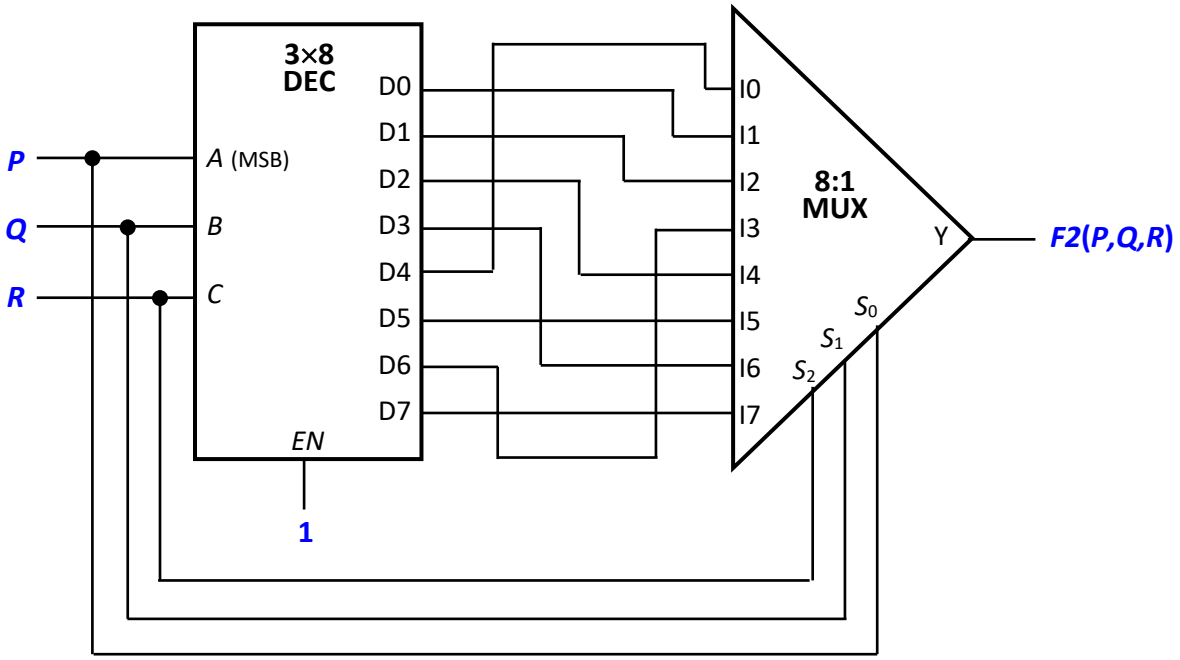


Figure 2

(a) Fill in the list of minterms for *F2*(*P*,*Q*,*R*) in the **Σm notation**, i.e. *F2*(*P*,*Q*,*R*) = $\Sigma m(\ldots)$. (1 mark)

(b) How many EPIs are there in the K-map of *F2*? (1 mark)

(c) You have seen this circuit (in another form) in class, what is the name of this circuit *F2*(*P*,*Q*,*R*)? (Give the name of the circuit, not a description of what it does.) (1 mark)

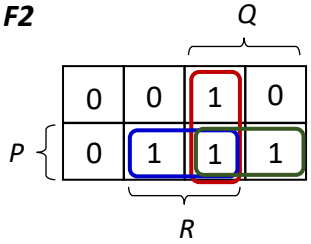
Answers:

(a) *F2*(*P*,*Q*,*R*) = $\Sigma m(\mathbf{3},\mathbf{5},\mathbf{6},\mathbf{7})$

(b) 3

(c) 3-bit majority logic circuit (lab 7)

P	*Q*	*R*	I0=D4	I1=D0	I2=D1	I3=D6	I4=D2	I5=D5	I6=D3	I7=D7	*Y*
0	0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	**1**	0	1
1	0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	**1**	0	0	1
1	1	0	0	0	0	**1**	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	**1**	1



Question 3. (Total: 4 marks)

Figure 3 below shows a function *F3*(*P*,*Q*,*R*) implemented using a 3×8 decoder with one-enable and active-high outputs and an 8:1 multiplexer.

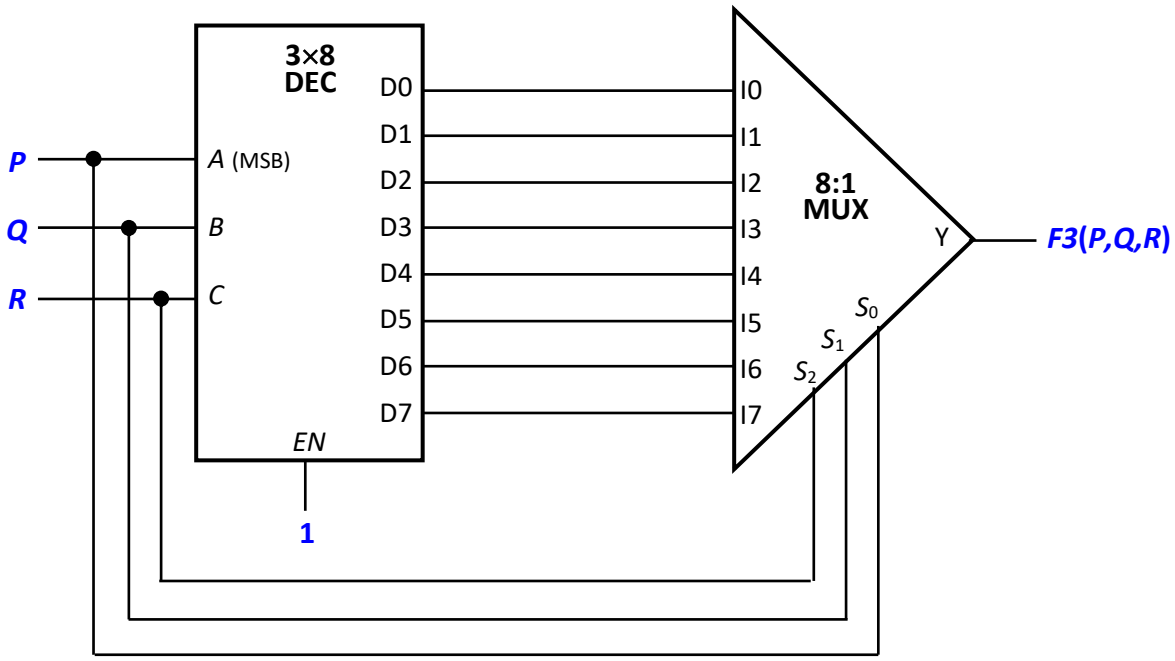


Figure 3

You are to replace the above circuit with a single 2-bit magnitude comparator as shown in Figure 4 below, without any additional logic gates.

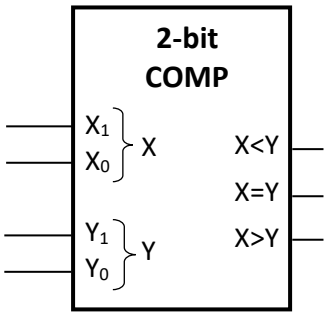


Figure 4

(a) Fill in the list of minterms for *F3*(*P*,*Q*,*R*) in the **Σm notation**, i.e. *F3*(*P*,*Q*,*R*) = $\Sigma m(\ldots)$. (1 mark)

(b) What is X? (1 mark)

(c) What is Y? (1 mark)

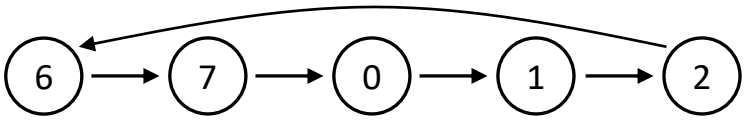
(d) Which output should be connected to *F3*? Is it X<Y or X=Y or X>Y? Do not add any space in your answer. (1 mark)

Answers:

(a) *F3*(*P*,*Q*,*R*) = $\Sigma m(\mathbf{0},\mathbf{2},\mathbf{5},\mathbf{7})$ (b) *PR* (c) *RP* (d) X=Y

Many alternative answers for (b) and (c). Check that the magnitude comparator returns 1 if and only if *P*=*R*. (Eg: *PP* and *RR*, 1*P* and 1*R*, *R*0 and *P*0, *QP* and *QR*, etc.)

Question 4. (Total: 3 marks)
A sequential circuit goes through the following states, whose state values are shown in decimal:



The states are represented by 3-bit values *ABC*. The sequential circuit is implemented using a *JK* flip-flop for *A*, a *T* flip-flop for *B*, and a *D* flip-flop for *C*. The block diagrams for all flip-flops are as given in the lecture slides.

(a) Two of the four flip-flop inputs have identical simplified SOP expressions. Write out the two flip-flop inputs, with an equal sign between them. Do not add any space. (For example, if you think that JA and KA are identical, then write "JA=KA" without the quotation marks.) (1 mark)

(b) Write the simplified SOP expression for DC. You do not need to write "DC=".

(For each product term in your SOP expression, write the literals in alphabetical order. Literals should be in upper-case letters, and there should be no spaces, no parentheses, and no symbols other than the dot, plus and single quote in your answer.) (1 mark)

(c) Apart from the flip-flops, what is the minimum number of logic gates required to implement the circuit? You do not need to follow the simplified SOP expressions in your implementation. (1 mark)

Answers:

(a) ***KA=TB*** or ***TB=KA***

(b) *DC*=***A·C'+B'·C'*** or ***B'·C'+A·C'***

(c) **2** logic gates or **1** logic gate

JA = B

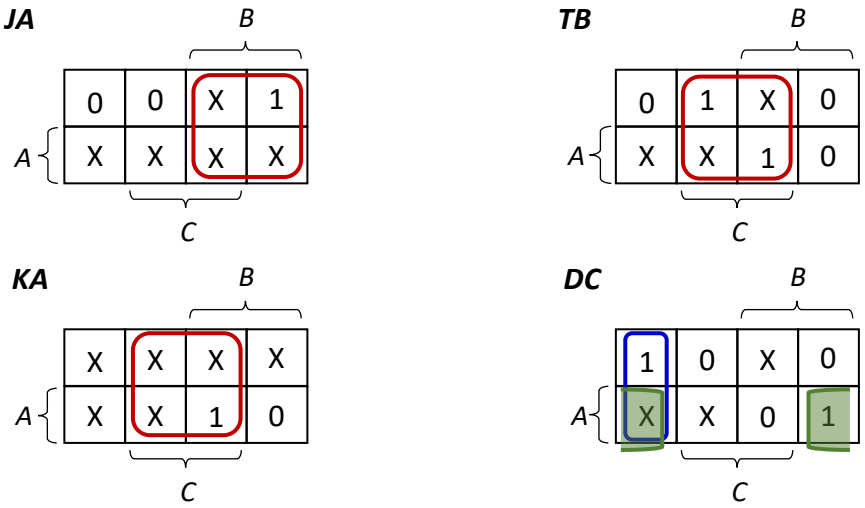
KA = TB = C

DC = A·C'+B'·C'

A	*B*	*C*	A^+	B^+	C^+	*JA*	*KA*	*TB*	*DC*
0	0	0	0	0	1	0	X	0	1
0	0	1	0	1	0	0	X	1	0
0	1	0	1	1	0	1	X	0	0
0	1	1	X	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X	X
1	0	1	X	X	X	X	X	X	X
1	1	0	1	1	1	X	0	0	1
1	1	1	0	0	0	X	1	1	0

2 logic gates: Rewrite *DC* as (*A*+*B'*) ·*C'*. As *B'* and *C'* are available from the *Q'* outputs of the flip-flops, hence only an OR gate and an AND gate are required.

1 logic gate: XNOR(A,B,C) = $\sum m(0,3,5,6)$ which covers *DC*. Although 3-input XNOR gates are rarely manufactured, it is theoretically correct.



Question 5. (Total: 7 marks)

The *LD* flip-flop shown in Figure 5 consists of two inputs *L* and *D*: when *L*=0 (load command), the next state Q^+ is set to *D*; when *L*=1 (toggle command), Q^+ is set to Q'.

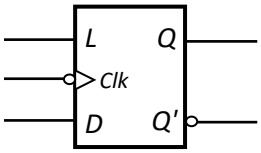


Figure 5

(a) Fill in the list of minterms for $Q^+(L,D,Q)$ in the **Σm notation**, i.e. $Q^+(L,D,Q) = \Sigma m(\dots)$. (1 mark)

(b) Suppose an *LD* flip-flop is at state 0. Let $T(L,D)$ be the function for the *LD* flip-flop to transit to next state 0. Write out the simplified SOP expression of $T(L,D)$. (1 mark)

(c) Suppose an *LD* flip-flop is at state 0. Let $U(L,D)$ be the function for the *LD* flip-flop to transit to next state 1. Write out the simplified SOP expression of $U(L,D)$. (1 mark)

For parts (d) to (g):

A sequential circuit with 4 states (represented by *AB*) and an external input *E* is implemented using two *LD* flip-flops. When *E*=0, the circuit cycles through the states 00, 01, 10, 11 and back to 00. When *E*=1, the next state is set to 10.

(d) Fill in the list of minterms for $A^+(A,B,E)$. (1 mark)

(e) What is the minimum number of logic gates needed to implement A^+? Logic gates that can be used are inverters, AND, OR, NAND, NOR, XOR and XNOR gates. Except for inverters, the rest are logic gates with fan-in of 2. (1 mark)

(f) Fill in the list of minterms for $B^+(A,B,E)$. (1 mark)

(g) What is the minimum number of logic gates needed to implement B^+? Logic gates that can be used are inverters, AND, OR, NAND, NOR, XOR and XNOR gates. Except for inverters, the rest are logic gates with fan-in of 2. (1 mark)

Answers:

(a) $Q^+(L,D,Q) = \Sigma m(\mathbf{2},\mathbf{3},\mathbf{4},\mathbf{6})$.

(b) $T(L,D)$ = ***L'·D'*** or ***D'·L'***
(Explanation: For the transition 0 to 0, *L*=0 and *D*=0.)

(c) $U(L,D)$ = ***L+D*** or ***D+L***
(Explanation: For the transition 0 to 1, (*L*=0 and *D*=1), or (*L*=1 and *D*=0), or (*L*=1 and *D*=1).)

(d) $A^+(A,B,E) = \Sigma m(\mathbf{1},\mathbf{2},\mathbf{3},\mathbf{4},\mathbf{5},\mathbf{7})$.

(e) **2** gates
(an XOR gate and an OR gate; $A^+ = E + (A \oplus B)$)

(f) $B^+(A,B,E) = \Sigma m(\mathbf{0},\mathbf{4})$.

(g) **1** gate (a NOR gate; $B^+ = (B+E)'$)

L	*D*	*Q*	Q^+
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

A	*B*	*E*	A^+	B^+
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	0

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