

Specifying and Reasoning Generic Architecture in TCOZ

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Abstract

Formal modeling techniques can be used to define and verify software architectures precisely. This paper applies the recently developed integrated formal specification techniques, Timed Communicating Object Z (TCOZ), to the generic software architecture modeling and verification.

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1 Introduction

Software architecture modeling is an important level of description for software systems. Z has been used to formalize the computational data/state aspects of software architectures [8]. CSP-like notation, Wright [1] has also been applied to formalize the interactive communication aspects of software architectures. Both approaches are beneficial and provide some formal foundations to software architecture description, however, the formal link and consistency issues between the models represented in different formalisms remain as a challenge. In this paper, we apply the integrated formal notation, Timed Communicating Object Z (TCOZ) [6], as an architecture description language (ADL) to model and verify a generic dispatch software system architecture. TCOZ builds on the strengths of Object-Z [2, 10] in modeling complex data and state with the strengths of TCSP [7] in modeling process control and real-time interactions. The class construct in TCOZ is an ideal encapsulation mechanism for composing and extending architecture models. The synchronized and asynchronized communication interfaces in TCOZ are well suited for capturing various interactions between the components. The network topology of TCOZ is a good mechanism to depicting the architectural configurations. Furthermore, TCOZ preserves a large part of both the syntax and semantics of the individual notations and hence can potentially benefit from existing reasoning systems of the individual nota-

tions. With some additional proof rules for the new TCOZ constructs, Smith's logic for Object-Z [9] (extension to the W logic of Z) and Davies/Schneider's proof system for TCSP [7] can be used for the reasoning of TCOZ properties, in this case the architecture model.

The dispatch system used in the paper (as a demonstrating example) is a generic system that provides automatic dispatching of the requested tasks. In this paper, we apply TCOZ to represent two layered architecture model of a generic dispatch system. These two layers include: an top level architectural style of the dispatch system and a generic timed-dispatch system architecture. The generic dispatch system assign the tasks within their critical timing requirements Critical system timing properties of the generic layer can be formulated and verified in TCOZ.

The main benefit of having a layered approach is reusability. The upper layers represent high abstraction of system architecture, i.e., generic patterns of components and connectors, so that high level relationships among system can be understood. The lower layer characterizes the specific domain, i.e., generic timing requirement and specific topology of components and connectors, This allows us to describe a system architecture as an open-ended collection of reusable architectural elements. Formal specifications of architecture models permit us to reason about important properties at each desired level.

The remainder of the paper is organized as follows. In section 2, we briefly introduce the TCOZ notation and its inference rules. Section 3 presents the architecture models of the generic dispatch system. Section 4 presents the verification of critical properties in the system. Section 5 concludes the paper.

2 TCOZ

Object-Z operation specification schemas with terminating CSP processes. Thus operation schemas and CSP processes occupy the same syntactic and semantic category; operation schema expressions can appear wherever

processes appear in CSP and CSP process definitions can appear wherever operation definitions appear in Object-Z. The primary specification structuring device in TCOZ is the Object-Z class mechanism.

In TCOZ, all timing information is represented as real valued measurements in e.g. *seconds*. We believe that a mature approach to measurement and measurement standards is essential to the application of formal techniques to system engineering problems. In order to support the use of standard units of measurement, extensions to the Z typing system suggested by Hayes and Mahony [3] are adopted. Under this convention, time quantities are represented by the type

$$\mathbb{T} ::= \mathbb{R} \odot \mathbb{T},$$

where \mathbb{R} represents the real numbers and \mathbb{T} is the SI symbol for dimensions of time. Time literals consist of a real number literal annotated with a symbol representing a unit of time. All the arithmetic operators are extended in the obvious way to allow calculations involving units of measurement.

2.1 Interface – channels, sensors and actuators

CSP channels are given an independent, first class role in TCOZ. In order to support the role of CSP channels, the state schema convention is extended to allow the declaration of communication channels. If c is to be used as a communication channel by any of the operations of a class, then it must be declared in the state schema to be of type **chan**. Channels are type heterogeneous and may carry communications of any type. Contrary to the conventions adopted for internal state attributes, channels are viewed as shared (global) rather than as encapsulated entities. This is an essential consequence of their role as communication interfaces *between* objects. The introduction of channels to TCOZ reduces the need to reference other classes in class definitions, thereby enhancing the modularity of system specifications.

Complementary to the synchronizing CSP channel mechanism, TCOZ also adopts a non-synchronizing shared variable mechanism. A declaration of the form $s : X$ **sensor** provides a channel-like interface for using the shared variable s as an input. A declaration of the form $s : X$ **actuator** provides a local-variable-like interface for using the shared variable s as an output. Sensors and actuators may appear either at the system boundary (usually describing how global analog quantities are sampled from, or generated by the digital subsystem) or else within the system (providing a convenient mechanism for describing local communications which do not require synchronization). We believe that TCOZ with the **actuator** and **sensor** can be a good candidate for specifying open control systems. Mahony and

Dong [5] presented a detailed discussion on TCOZ sensor and actuators.

2.2 Active objects, semantics and network topologies

Active objects have their own thread of control, while passive objects are controlled by other objects in a system. In TCOZ, an identifier **MAIN** (non-terminating process) is used to determine the behavior of active objects of a given class. The **MAIN** operation is optional in a class definition. It only appears in a class definition when the objects of that class are active objects. Classes for defining passive objects will not have the **MAIN** definition, but may contain CSP process constructors. If ob_1 and ob_2 are active objects of the class C , then the independent parallel composition behavior of the two objects can be represented as $ob_1 \parallel ob_2$, which means $ob_1.MAIN \parallel ob_2.MAIN$

The details of the blended state/event process model forms the basis for the TCOZ semantics [4]. In brief, the semantic approach identifies the notions of operation and process by providing a process interpretation of the Z operation schema construct. TCOZ differs from many other approaches to blending Object-Z with a process algebra in that it does not identify operations with events. Instead an unspecified, fine-grained collection of state-update events is hypothesized. Operation schemas are modeled by the collection of those sequences of update events that achieve the state change described by the schema. This means that there is no semantic difference between a Z operation schema and a CSP process. It therefore makes sense to also identify their syntactic classes.

The syntactic structure of the CSP synchronization operator is more suitable in the case of pipeline like communication topologies. When expressing more complex communication topologies it generally results in unacceptably complicated expressions. In TCOZ, a graph-based approach is adopted to represent the network topology [6]. For example, consider that processes A and B communicate privately through the interface ab , processes A and C communicate privately through the interface ac , and processes B and C communicate privately through the interface bc . This network topology of A , B and C may be described by

$$\parallel (A \xleftrightarrow{ab} B; B \xleftrightarrow{bc} C; C \xleftrightarrow{ca} A).$$

Other forms of lax usage allow network connections with common nodes to be run together, for example

$$\parallel (A \xleftrightarrow{ab} B \xleftrightarrow{bc} C \xleftrightarrow{ca} A),$$

and multiple channels above the arrow, for example if processes D and F communicate privately through the channel/sensor-actuator df_1 and df_2 , then

$$\parallel (D \xleftrightarrow{df_1, df_2} F).$$

2.3 TCOZ inference rules

The proof facilities of Object-Z and TCSP can be used to the reasoning of both state and event oriented properties of a TCOZ specification.

2.3.1 State aspects reasoning

The essential extension to Z in Object-Z is the class construct which groups the definition of a state schema and the definitions of its associated operations. From a system point of view, it also enables modular verification. Smith [9] extends the *W* logic of Z to Object-Z in reasoning about object orientation, i.e., the class constructs. The fundamental logic in Object-Z is the sequent defined as follows:

$$A :: d \mid \Psi \vdash \Phi$$

where *A* is the name of a class, *d* is a list of declarations and Ψ and Φ are list of predicates in the local content of class *A*. Inference rules are also restricted in the local environment of a class context.

$$\frac{A :: d_1 \mid \Psi_1 \vdash \Phi_1}{A :: d_2 \mid \Psi_2 \vdash \Phi_2} [A :: p]$$

The upper part is called a premiss which contains zero or more sequents; the middle part is called a proviso which is a predicate that makes the rule applicable; and the lower part is called a conclusion which is a single sequent which must be valid when the proviso and the premisses are true. A detailed information of Object-Z inference rules can be found in Smith's logic for Object-Z [9].

2.3.2 TCOZ extension rules

TCOZ [6] extends Object-Z class definition in two aspects. Firstly, the state schema convention is extended to allow the declaration of object communication interfaces, i.e., channels, sensors and actuators. If *c* is to be used as a communication interface by any of the operations of a class, then it must be explicitly declared in the state schema. Channels are type heterogeneous and may carry communications of any type, while sensor/actuators are type specific. These communication interfaces are connected by the network topologies in TCOZ. The second extension is that as well as operations (terminating processes), non-terminating processes named *MAIN* are introduced to represent the behavior of active classes. The inheritance mechanism of active classes differs from the normal passive classes as the *MAIN* operation must always be redefined explicitly. Based on the logic of Object-Z, additional rules are introduced for the manipulating of the new TCOZ type constructs such as **chan**, **sensor** and **actuator**.

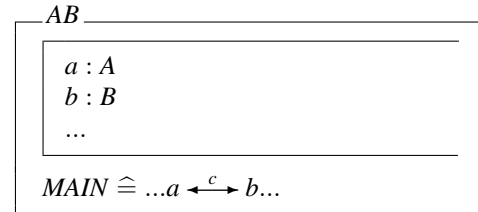
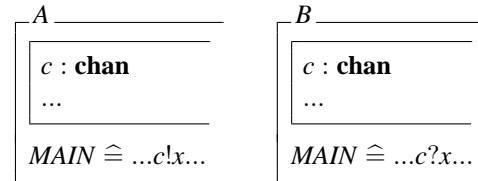
- Non-terminating process (*MAIN*) – For a generic *MAIN* definition of class $A[X_1, \dots, X_n]$, the inference rule is defined as follows:

$$MAIN \hat{=} OP$$

$$\frac{A[t_1, \dots, t_n] :: MAIN = \Delta STATE \bullet (b \odot OP) \vdash}{A[t_1, \dots, t_n] :: \vdash} [q]$$

MAIN refers to the non-terminating process definition in an active class. Note that there is no need to consider the inherited *MAIN* definitions from its super-classes since the process *MAIN* must always be redefined in the subclasses if it appears. The proviso *q* is in the form of $q \equiv b = (\bigwedge X_1 \rightsquigarrow t_1, \dots, X_n \rightsquigarrow t_n)$.

- Synchronized communication (Channel) – For a generic network topology definition of classes *A*, *B* and *AB*, the channel inference rule is defined as follows:



$$\frac{\begin{array}{l} A[t_1, \dots, t_n] :: STATE \vdash c \in \mathbf{chan} \\ \quad \wedge MAIN \vdash c!x \in X \\ B[t_1, \dots, t_n] :: STATE \vdash c \in \mathbf{chan} \\ AB[t_1, \dots, t_n] :: STATE \vdash a \in A \wedge b \in B \\ \quad \wedge MAIN \vdash a \xleftrightarrow{c} b \end{array}}{B[t_1, \dots, t_n] :: MAIN \vdash c.x \in X} [q]$$

The above states that if class *A* and *B* are communicating through channel *c*, synchronization will be enforced on the input and outputs, i.e., outputs from *A* through *c* will lead to inputs to *B*.

2.3.3 Timed event aspects reasoning

TCSP [7] is an extension to Hoare's Communicating Sequential Process (CSP) to accommodate the description of time-sensitive behaviors. A requirements specification

$$\text{MAIN} \hat{=} \mu R \bullet [r : \text{ReportInfo}; a : \text{AuxInfo}, \\ t : \text{Task}] \bullet \text{listenport?}(\text{self}, r) \rightarrow (\text{synauxport?} \\ (\text{self}, a) \rightarrow \text{SKIP} \square \text{asynauxport?}(\text{self}, a) \\ \rightarrow \text{SKIP}); \text{reportport!}t \rightarrow \text{SKIP}; R$$

ControlUnit

$$\text{reportport} : \mathbf{chan} \\ \text{dispatchport} : \mathbf{chan}$$

$$\text{MAIN} \hat{=} \mu C \bullet ([t : \text{Task}] \bullet \text{reportport?}t \rightarrow \\ \text{SKIP}) \square ([t : \text{tasks}, e : \text{ExecuteUnit}] \bullet \\ \text{dispatchport!}(e, t) \rightarrow \text{SKIP}); C$$

ExecuteUnit

$$\text{dispatchport} : \mathbf{chan}$$

$$\text{MAIN} \hat{=} \mu E \bullet [t : \text{Task}] \bullet \text{dispatchport?}(\text{self}, t) \\ \rightarrow \text{SKIP}; E$$

AuxiliaryUnit[X]

$$\text{synauxport} : \mathbf{chan} \\ \text{asynauxport} : X \mathbf{actuator}$$

$$\text{MAIN} \hat{=} \mu A \bullet [a : \text{AuxInfo}, r : \text{ReportUnit}] \bullet \\ ((\text{synauxport!}(r, a) \rightarrow \text{SKIP}) \square \\ (\text{asynauxport!}(r, a) \rightarrow \text{SKIP})); A$$

Note that the communications between *ReportUnit* and *AuxUnit* may be synchronous or asynchronous. Each component has its own interfaces for communication with the rest of the system. For example, the component *ControlUnit* has two communication interfaces: *reportport* and *dispatchport*. When data is received by *ControlUnit* through the *reportport*, it is processed and then sent out through the *dispatchport* after processing. The details of encapsulated behaviors of the components are deliberately suppressed here in the architectural style since each component of the same type may have different computation behaviors. In the MAIN operation of each component, we defines the communication patterns. However, according to TCOZ semantics for inheritance, all MAIN operations will be explicitly redefined when this level of style is inherited and extended for a particular system. In the TCOZ approach, system configurations are specified in network topology.

DispatchSys[X]

$$c : \downarrow \text{ControlUnit} \\ rs : \mathbb{F}_1 \downarrow \text{ReportUnit}[X] \\ es : \mathbb{F}_1 \downarrow \text{ExecuteUnit} \\ as : \mathbb{F} \downarrow \text{AuxiliaryUnit}[X]$$

$$\text{MAIN} \hat{=} \parallel_{(a,r,e):as \times rs \times es} \\ (a \xrightarrow{\text{synauxport, asynauxport}} r \xrightarrow{\text{reportport}} c \xrightarrow{\text{dispatchport}} e)$$

The network topology expression clearly identifies the interaction range of each component. For example, the *ControlUnit* communicates with *ReportUnits* through the *reportport* while it communicates with *ExecuteUnits* through the *dispatchport*. Note that ‘ \downarrow ’ is the standard polymorphic type constructor in Object-Z language. More importantly, the TCOZ reuse mechanisms (inheritance and instantiation) allows the architecture style models to be extended to build generic and specific system architecture models, which will be shown in later sub-sections.

3.2 A Generic Architecture for the Timed Dispatch System

In this section, we will present a generic architecture of the timed dispatch system specified in TCOZ. We inherit, extend and instantiate the architectural style presented in the previous section. Unlike the style, a generic model defines crucial timing computation and communication details of the components in the system. Following the architectural style, we decompose the system into three main types of components (not including auxiliary components):

- The central dispatcher stores the tasks, updates the tasks and dispatches tasks to related task executers according to the business logic.
- The emergency report receivers obtain emergency information, create tasks and send the tasks to the central dispatcher.
- The task executers execute the tasks dispatched to them. The role of executers may vary in different Dispatch Systems, such as police offices in police system, hospitals in medical system, etc.

Clock and *Log*, two auxiliary components in the model, offer time information and logging of important system actions respectively. The subscriber’s role also vary in different systems, from patients in the medical system to case locations in the police system. Since most Dispatch Systems are time-critical, we make the timing requirement an important feature in our generic model. Furthermore, some

$| \text{Task}_T : \text{Task} \rightarrow \mathbb{T}$

A generic function pt (purge task) is defined to purge the time out items from the original set into the second set corresponding to the time elapsed and update the time stamps accordingly:

$$\begin{array}{l} \overline{\overline{[X]}} \\ pt : (\mathbb{T} \times \mathbb{F}(X \times \mathbb{T})) \rightarrow (\mathbb{F}(X \times \mathbb{T}) \times \mathbb{F}X) \\ \forall t : \mathbb{T}; s : \mathbb{F}(X \times \mathbb{T}) \bullet pt(t, s) = (\{(e, t_o) : s \mid \\ t_o > t \bullet (e, t_o - t)\}, \{(e, t_o) : s \mid t_o \leq t \bullet e\}) \end{array}$$

e.g.

$$pt(2\mathbf{s}, \{(a, 1\mathbf{s}), (b, 3\mathbf{s}), (c, 7\mathbf{s})\}) = \\ (\{(b, 1\mathbf{s}), (c, 5\mathbf{s})\}, \{a\})$$

which means that after the elapsing of 2 seconds the time stamp of b and c would become 1 and 5, and the time out item a is purged into the second set.

The most critical system component is the *Dispatcher* class:

$$\begin{array}{l} \overline{\text{Dispatcher}} \\ \text{ControlUnit}[\text{login/reportport}, \text{dispatch/dispatchport}] \\ \hline ex : \mathbb{F}_1 \text{Executer} \\ tasks : \mathbb{F}(\text{Task} \times \mathbb{T}) \\ \Delta \\ t : \mathbb{T}; \text{timeup} : \mathbb{F} \text{Task} \\ \hline tasks \neq \emptyset \Rightarrow 0 \leq t \leq \min \text{ran } tasks \\ \hline \text{INIT} \\ tasks = \emptyset \\ \hline \text{Add} \\ \Delta(tasks) \\ task? : \text{Task}; t_i? : \mathbb{T} \\ \hline task' = \text{fst}(pt(t_i?, tasks)) \cup (task?, \text{Task}_T(task?)) \\ \text{timeup}' = \text{snd}(pt(t_i?, tasks)) \\ \hline \text{Purge} \\ \Delta(tasks) \\ \hline pt(t, tasks) = (tasks', \text{timeup}') \\ \hline \text{AddTask} \hat{=} [task : (\text{Task} - \text{dom } tasks); t_i : \mathbb{T}] \bullet \\ \text{login?}task@t_i \rightarrow \text{Add} \\ \text{Dispatch} \hat{=} [f : \text{timeup} \rightarrow ex] \bullet \\ \text{|||}_{(task, e):f} \text{dispatch!}(e, task) \rightarrow \text{SKIP} \\ \text{MAIN} \hat{=} \mu D \bullet ([tasks = \emptyset] \bullet \text{AddTask} \square [tasks \neq \emptyset] \bullet \\ (\text{AddTask} \triangleright \{t\} (\text{Purge}; \text{Dispatch}))); D \end{array}$$

Secondary attribute t records the time value which is less than or equal to the minimum time stamp in the task set. This constraint is captured by the class invariant, which must be preserved by all operations. Attribute *timeup* stores all the time-out tasks after each purge operation.

The behavior of the MAIN process of the dispatcher is basically either adding or dispatching tasks. If the task set is empty, only adding is performed; while for the non-empty task set, both adding and dispatching are enabled.

The overall system is a composition of all components that communicate with each other. We organize the interactive components through network topologies.

$$\begin{array}{l} \overline{\text{TimedDispatchSys}} \\ \text{DispatchSys}[\text{CalT}][d/c] \\ \hline \text{clock} : \text{Clock} \\ \text{inlog} : \text{Log}[\text{CalT} \times \text{Task}] \\ \text{dispatchlog} : \text{Log}[\text{CalT} \times \text{Task} \times \text{Executer}] \\ \hline d \in \text{Dispatcher} \wedge d.ex = es \\ \forall r : rs \bullet r \in \text{Receiver} \\ \forall e : es \bullet e \in \text{Executer} \\ \{\text{clock}, \text{inlog}, \text{dispatchlog}\} \subseteq as \\ \hline \text{MAIN} \hat{=} \text{|||}_{(r, e):rs \times es} (r \xrightarrow{\text{login}} d \xrightarrow{\text{dispatch}} e; \\ \text{inlog} \xrightarrow{\text{record}} r \xrightarrow{\text{time}} \text{clock} \xrightarrow{\text{time}} e \xrightarrow{\text{record}} \text{dispatchlog}) \end{array}$$

4 Analysis and Reasoning

From a safety critical perspective, the key point of the Dispatch system is to provide guaranteed time critical service to all the valid tasks. This critical property can be formally interpreted from our model as:

$$\begin{array}{l} \text{Thm: } \text{TimedDispatchSys} \bullet \forall task_o : \text{Task}; ct_1 : \text{CalT} \bullet \\ (ct_1, task_o) \in \text{ran } \text{inlog.log} \Rightarrow \exists ct_2 : \text{CalT}; e : es \bullet \\ (ct_2, task_o, e) \in \text{ran } \text{dispatchlog.log} \wedge \\ (\text{cal}^\sim(ct_2) - \text{cal}^\sim(ct_1)) \leq \text{Task}_T(task_o) \end{array} \quad [P]$$

The above simply states that any task which logged into the system will be dispatched within its critical time requirement. To prove the validity of the theorem P , the first thing is to show that the *Clock* component in our system correctly models the behavior of a physical timing device – the global clock. This property can be interpreted into the following timed specification in terms of the timed failure model.

$$\begin{array}{l} \text{Lemma: } L_0(s, \aleph) = \text{Clock} :: \forall total : \mathbb{N}\mathbf{s}; t_0 : \mathbb{T} \bullet \\ \text{time!cal}(total) \text{ at } t_0 \Rightarrow \text{time!cal}(total') \text{ at } (t_0 + 1\mathbf{s}) \end{array}$$

Proof:

Base case: The specification is trivially satisfied by *STOP*.

Assuming the $C \text{ sat } L_0(s, \aleph)$, it is sufficient to show that $(Inc \bullet \text{DEADLINE } 50 \text{ ms}) \bullet \text{WAITUNTIL } 1 \text{ s}; C \text{ sat } L_0(s, \aleph)$.

Let:

$$\begin{aligned} L_1(s, \aleph) &= \text{Clock} :: \forall total : \mathbb{N} \mathbf{s}; t_0 : \mathbb{T} \bullet \text{time!cal}(total) \\ &\quad \text{at } t_0 \Rightarrow \text{time!cal}(total') \text{ at } [t_0, \infty) \\ L_2(s, \aleph) &= \text{Clock} :: \forall total : \mathbb{N} \mathbf{s}; t_0 : \mathbb{T} \bullet \text{time!cal}(total) \\ &\quad \text{at } t_0 \Rightarrow \text{time!cal}(total') \text{ at } [t_0, t_0 + 50 \text{ ms}] \end{aligned}$$

The proof of $[L_0]$ can be constructed as follows:

$$\begin{array}{c} \frac{\text{Clock} :: Inc \text{ sat } L_1(s, \aleph)}{[\text{DEADLINE}]} \\ \frac{\text{Clock} :: Inc \bullet \text{DEADLINE } 50 \text{ ms} \text{ sat} \\ \quad (end(s) \leq 50 \text{ ms} \wedge \checkmark \in \sigma(s) \wedge \\ \quad L_1(s, \aleph \upharpoonright 50 \text{ ms}))}{[\text{Weaken}]} \\ \frac{\text{Clock} :: Inc \bullet \text{DEADLINE } 50 \text{ ms} \text{ sat} \\ \quad L_2(s, \aleph)}{[\text{WAITUNTIL}]} \\ \frac{\text{Clock} :: (Inc \bullet \text{DEADLINE } 50 \text{ ms}) \bullet \\ \quad \text{WAITUNTIL } 1 \text{ s} \text{ sat} \\ \quad ((end(s) > 1 \text{ s} \wedge \\ \quad L_2(s, \aleph)) \vee \\ \quad (end(s) \leq 1 \text{ s} \wedge L_2(s, \aleph) \\ \quad \wedge \checkmark \text{ live from } 1 \text{ s} \text{ until } \{\checkmark\}))}{[\text{Weaken}]} \\ \frac{\text{Clock} :: (Inc \bullet \text{DEADLINE } 50 \text{ ms}) \bullet \\ \quad \text{WAITUNTIL } 1 \text{ s} \text{ sat } L_0(s, \aleph)}{[\text{Composition}]} \\ \frac{\text{Clock} :: ((Inc \bullet \text{DEADLINE } 50 \text{ ms}) \bullet \\ \quad \text{WAITUNTIL } 1 \text{ s}); C \text{ sat} \\ \quad ((\checkmark \notin \sigma(s) \wedge \\ \quad L_0(s, \aleph \cup [0, \infty) \times \{\checkmark\})) \\ \quad \vee (\exists s_1, s_2 \bullet s = s_1 \hat{\ } s_2 \\ \quad \wedge \checkmark \notin \sigma(s_1) \wedge \\ \quad \text{begin}(s_1) \geq t \wedge \\ \quad L_0(s_1 \hat{\ } \langle (t, \checkmark) \rangle, \\ \quad \aleph \upharpoonright t \cup [0, t) \times \{\checkmark\}) \wedge \\ \quad L_0((s_2, \aleph) - t)))}{[\text{Weaken}]} \\ \text{Clock} :: ((Inc \bullet \text{DEADLINE } 50 \text{ ms}) \bullet \\ \quad \text{WAITUNTIL } 1 \text{ s}); C \text{ sat } L_0(s, \aleph) \end{array}$$

According to the recursion induction rule, the behavior specification $L_0(s, \aleph)$ is satisfied, therefore **Lemma** L_0 has been proved.

After showing that the *Clock* component is consistent to the global clock, we now can decompose the theorem P into state-based properties and event/time-based properties as follows:

- No message lost – This property claims that no tasks will be lost once they are in the system. It can be translated into the statement that any task in the login log would be eventually in the dispatched log:

$$\begin{aligned} \text{Thm 1: } \text{TimedDispatchSys} &:: \forall task : \text{Task} \bullet \\ &\quad task \in \text{ran ran } inlog.log \Rightarrow \\ &\quad task \in \text{ran ran } dispatchlog.log \quad [P_1] \end{aligned}$$

- Dispatching within critical time range – This property claims that all tasks in the system will be dispatched to a execution unit at their required critical time range. It can be translated into the statement that the duration from login the system to its dispatch of each task should be exactly equal to its time requirement $Task_T(task)$:

$$\begin{aligned} \text{Thm 2: } \text{TimedDispatchSys} &:: \forall task : \text{Task}; \\ &\quad t_0 : \mathbb{T}; e : es \bullet \text{login?task at } t_0 \Rightarrow \\ &\quad \text{dispatch!}(e, task) \text{ at } (t_0, t_0 + Task_T(task)) \quad [P_2] \end{aligned}$$

As from above, theorem P can be formally decomposed into data (state-based) property P_1 and timing (event-based) property P_2 , which later can be proved by the combination of Object-Z and TCSP's inference systems respectively.

4.1 Proof of P_1

First, we use induction to prove the following property holds by the *Dispatcher* class.

$$\begin{aligned} \text{Theorem 3: } \text{Dispatcher} &:: \forall task : \text{Task} \bullet \\ &\quad (task, Task_T(task)) \in \text{tasks} \Rightarrow \\ &\quad \text{dispatch.}(e, task) \in (\text{Executer} \times \text{Task}) \quad [P_3] \end{aligned}$$

Proof:

Initially: $\text{Dispatcher} :: \text{INIT} \vdash \text{tasks} = \emptyset$, therefore predicate $[P_3]$ holds (trivial).

Assume the pre-state of the operations in class *Dispatcher* is true, which is $[\forall task : \text{Task} \bullet (task, Task_T(task)) \in \text{tasks} \Rightarrow \text{dispatch.}(e, task) \in (\text{Executer} \times \text{Task})]$. The post-state of *Dispatcher* is depicted by two kinds of behaviors, *AddTask* and *(Purge; Dispatch)*, which associated with the timeout constraint as follows:

- If no new task is added after the minimum time stamp of all tasks – t , the *(Purge; Dispatch)* operation will perform, which will reduce the number of tasks in the *tasks* set. According to the assumption, $[P_3]$ holds for the post-state.
- If a new task is added to the *tasks* set before t , by the definition of the *pt* function, the time stamp of this particular task will monotonously decrease as either the

AddTask or (*Purge*; *Dispatch*) operation would perform. Thus the task will eventually be purged from the *tasks* set and dispatched to the *Executors*. Therefore, $[P_3]$ holds for the post-state.

According to the structured induction, **Theorem P_3** is proved.

The proof of $[P_1]$ can be constructed via state reasoning rules as follows:

$$\begin{array}{l}
\textit{TimedDispatchSys} :: \textit{STATE} \vdash d \in \textit{Dispatcher} \wedge \\
\quad rs \in \mathbb{F}_1 \textit{Receiver} \wedge \textit{inlog} \in \textit{Log}[\textit{CalT} \times \textit{Task}] \\
\textit{Receiver} :: \textit{STATE} \vdash \textit{listen}, \textit{login}, \textit{record} \in \mathbf{chan} \wedge \\
\quad \textit{MAIN} \vdash \textit{listen.task} \in \textit{Task} \Rightarrow \textit{login.task} \in \textit{Task} \\
\quad \wedge \textit{record}.(t, \textit{task}) \in \textit{CalT} \times \textit{Task} \\
\textit{Dispatcher} :: \textit{STATE} \vdash \textit{login} \in \mathbf{chan} \\
\textit{Log}[\textit{CalT} \times \textit{Task}] :: \textit{STATE} \vdash \textit{record} \in \mathbf{chan} \\
\textit{TimedDispatchSys} :: \textit{MAIN} \vdash r \in rs \wedge \\
\quad d \xrightarrow{\textit{login}} r \xrightarrow{\textit{record}} \textit{inlog} \\
\hline
\textit{Dispatcher} :: \textit{MAIN} \vdash \textit{login.task} \in \textit{Task} \Rightarrow \\
\quad (\textit{task}, \textit{Task}_T(\textit{task})) \in \textit{tasks} \wedge \\
\textit{Log}[\textit{CalT} \times \textit{Task}] :: \textit{MAIN} \vdash \\
\quad \textit{record}.(t, \textit{task}) \in \textit{CalT} \times \textit{Task} \Rightarrow \\
\quad (t, \textit{task}) \in \textit{ran log}
\end{array}$$

$$\begin{array}{l}
\textit{TimedDispatchSys} :: \textit{STATE} \vdash d \in \textit{Dispatcher} \wedge \\
\quad es \in \mathbb{F}_1 \textit{Executor} \wedge \textit{dipatchlog} \in \\
\quad \textit{Log}[\textit{CalT} \times \textit{Task} \times \textit{Executor}] \\
\textit{Dispatcher} :: \textit{MAIN} \vdash \textit{login.task} \in \textit{Task} \Rightarrow \\
\quad (\textit{task}, \textit{Task}_T(\textit{task})) \in \textit{tasks} \\
\textit{Dispatcher} :: \textit{STATE} \vdash \textit{dispatch} \in \mathbf{chan} \\
\textit{Dispatcher} :: \vdash (\textit{task}, \textit{Task}_T(\textit{task})) \in \textit{tasks} \Rightarrow \\
\quad \textit{dispatch}.(e, \textit{task}) \in \textit{Executor} \times \textit{Task} \\
\textit{Executor} :: \textit{STATE} \vdash \textit{dispatch} \in \mathbf{chan} \\
\textit{DispatchSysyem} :: \textit{MAIN} \vdash e \in es \wedge d \xrightarrow{\textit{dispatch}} e \\
\hline
\textit{Executor} :: \textit{MAIN} \vdash \textit{dispatch}.(e, \textit{task}) \in \textit{Executor} \times \textit{Task} \\
\hline
\textit{Executor} :: \textit{STATE} \vdash \textit{record} \in \mathbf{chan} \wedge \textit{MAIN} \vdash \\
\quad \textit{dispatch}.(e, \textit{task}) \in \textit{Executor} \times \textit{Task} \Rightarrow \\
\quad \textit{record}.(t, \textit{task}, \textit{self}) \in \textit{CalT} \times \textit{Task} \times \textit{Executor} \\
\textit{Log}[\textit{CalT} \times \textit{Task} \times \textit{Executor}] :: \textit{STATE} \vdash \textit{record} \in \mathbf{chan} \\
\textit{DispatchSysyem} :: \textit{MAIN} \vdash e \in es \wedge e \xrightarrow{\textit{record}} \textit{dispatchlog} \\
\hline
\textit{Log}[\textit{CalT} \times \textit{Task} \times \textit{Executor}] :: \textit{MAIN} \vdash \\
\quad \textit{record}.(t, \textit{task}, e) \in \textit{CalT} \times \textit{Task} \times \textit{Executor} \Rightarrow \\
\quad (t, \textit{task}, e) \in \textit{ran log}
\end{array}$$

Thus P_1 can be clearly derived from $P_{1.1}$ and $P_{1.2}$ as fol-

lows:

$$\begin{array}{l}
\textit{TimedDispatchSys} :: \textit{STATE} \vdash \textit{inlog} \in \textit{Log}[\textit{CalT} \times \textit{Task}] \\
\quad \wedge \textit{dipatchlog} \in \textit{Log}[\textit{CalT} \times \textit{Task} \times \textit{Executor}] \\
\textit{Log}[\textit{CalT} \times \textit{Task}] :: \textit{MAIN} \vdash \\
\quad \textit{record}.(t, \textit{task}) \in \textit{CalT} \times \textit{Task} \Rightarrow (t, \textit{task}) \in \textit{ran log} \\
\textit{Log}[\textit{CalT} \times \textit{Task} \times \textit{Executor}] :: \textit{MAIN} \vdash \\
\quad \textit{record}.(t, \textit{task}, e) \in \textit{CalT} \times \textit{Task} \times \textit{Executor} \Rightarrow \\
\quad (t, \textit{task}, e) \in \textit{ran log} \\
\hline
\end{array}$$

$$\begin{array}{l}
\textit{TimedDispatchSys} :: \vdash \forall \textit{task} : \textit{Task} \bullet \\
\quad \textit{task} \in \textit{ran ran inlog.log} \Rightarrow \\
\quad \textit{task} \in \textit{ran ran dipatchlog.log}
\end{array}$$

4.2 Proof of P_2

P_2 can be interpreted as the following timed specification in terms of the timed failure model.

$$P_2(s, \aleph) = \textit{Dispatcher} :: \forall \textit{task} : \textit{Task}; t_0 : \mathbb{T}; e : es \bullet \\
\quad \textit{login}? \textit{task} \textit{ at } t_0 \Rightarrow \textit{dispatch}!(e, \textit{task}) \textit{ at } \\
\quad (t_0, t_0 + \textit{Task}_T(\textit{task}))$$

Proof:

Base case: The specification is trivially satisfied by *STOP*.

Assuming the $D \text{ sat } P_2(s, \aleph)$, it is sufficient to show that $([\textit{tasks} = \emptyset] \bullet \textit{AddTask} \square [\textit{tasks} \neq \emptyset] \bullet \textit{AddTask} \triangleright \{t\} (\textit{Purge}; \textit{Dispatch}))$; $D \text{ sat } P_2(s, \aleph)$.

Let $P_{2.1}, P_{2.2}$ be two parts of the timeout primitive in P_2 as follows:

$$\begin{array}{l}
P_{2.1}(s, \aleph) = \textit{Dispatcher} :: \forall \textit{task} : \textit{Task}; t_0 : \mathbb{T}; e : es \bullet \\
\quad \textit{login}? \textit{task} \textit{ at } t_0 \Rightarrow t_0 < t \wedge \textit{timeup} = \emptyset \wedge \\
\quad \neg (\textit{dispatch}!(e, \textit{task}) \textit{ at } t_0) \\
P_{2.2}(s, \aleph) = \textit{Dispatcher} :: \forall \textit{task} : \textit{Task}; t_0 : \mathbb{T}; e : es \bullet \\
\quad (\textit{dispatch}!(e, \textit{task}) \textit{ at } t_0 \Rightarrow t_0 = t \wedge \textit{timeup} \neq \emptyset \wedge \\
\quad \exists ts \subseteq \textit{tasks} \bullet \forall (\textit{task}_1, t_1), (\textit{task}_2, t_2) \in ts \bullet \\
\quad t_1 = t_2 = t \wedge \textit{Task}_T(\textit{task}_1) = \textit{Task}_T(\textit{task}_2))
\end{array}$$

From the definition of function *pt*, *Add* and *Purge* operations, it is trivial to show that $P_{2.1}$ and $P_{2.2}$ are satisfied by *AddTask* and (*Purge*; *Dispatch*) respectively. The proof of $[P_2]$ can be constructed via event reasoning rules as follows:

$$\begin{array}{l}
\text{Dispatcher} :: ([tasks \neq \emptyset] \bullet \text{AddTask}) \text{ sat } P_{2.1}(s, \aleph) \\
\text{Dispatcher} :: ([tasks \neq \emptyset] \bullet (\text{Purge}; \text{Dispatch})) \\
\quad \text{sat } P_{2.2}(s, \aleph) \\
\hline
\text{Dispatcher} :: ([tasks \neq \emptyset] \bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \\
\text{Dispatch})) \text{ sat } (\text{begin}(s) < t \wedge P_{2.1}(s, \aleph)) \\
\vee (\text{begin}(s) \geq t \wedge P_{2.1}(\langle \rangle, \aleph \upharpoonright t) \wedge \\
P_{2.2}((s, \aleph) - t)) \\
\hline
\text{Dispatcher} :: ([tasks \neq \emptyset] \bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \\
\text{Dispatch})) \text{ sat } P_2(s, \aleph) \\
\text{Dispatcher} :: ([tasks = \emptyset] \bullet \text{AddTask}) \text{ sat } P_2(s, \aleph) \\
\hline
\text{Dispatcher} :: ([tasks = \emptyset] \bullet \text{AddTask} \square [tasks \neq \emptyset] \\
\bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \text{Dispatch})) \text{ sat } P_2(s, \aleph) \\
\wedge P_2(\langle \rangle, \aleph \upharpoonright \text{begin}(s)) \\
\hline
\text{Dispatcher} :: ([tasks = \emptyset] \bullet \text{AddTask} \square [tasks \neq \emptyset] \\
\bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \text{Dispatch})) \text{ sat } P_2(s, \aleph) \\
\text{Dispatcher} :: D \text{ sat } P_2(s, \aleph) \\
\hline
\text{Dispatcher} :: ([tasks = \emptyset] \bullet \text{AddTask} \square [tasks \neq \emptyset] \\
\bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \text{Dispatch})); D \text{ sat} \\
\checkmark \notin \sigma(s) \wedge P_2(s, \aleph \cup [0, \infty) \times \{\checkmark\}) \\
\vee \exists s_1, s_2, d \bullet s = s_1 \hat{\ } s_2 \wedge \checkmark \notin \sigma(s_1) \wedge \\
P_2(s_1 \hat{\ } \langle (d, \checkmark) \rangle, \aleph \upharpoonright d \cup [0, d) \times \{\checkmark\}) \wedge \\
P_2((s_2, \aleph) - d) \\
\hline
\text{Dispatcher} :: ([tasks = \emptyset] \bullet \text{AddTask} \square [tasks \neq \emptyset] \\
\bullet \text{AddTask} \triangleright \{t\} (\text{Purge}; \text{Dispatch})); D \\
\text{sat } P_2(s, \aleph)
\end{array}$$

According to the recursion induction rule, the behavior specification $P_2(s, \aleph)$ is satisfied, therefore **Theorem** P_2 has been proved. Thus the critical requirements of the timed dispatch system architecture are formally verified.

5 Conclusions

In this paper, we have applied the integrated formal notation TCOZ [6] as an ADL to the design and verification of an incremental two layer architecture model for the dispatch system architecture, i.e., the style and the timed generalization. The dispatch style captures the most common patterns among the dispatch systems. The generalization layer models the essential functionalities of the timed dispatch systems. Thus new systems are built as variations and customizations of the up-level designs, and the whole architecture is depicted as an open-ended design for reuse. In this paper, we also found that TCOZ could be a potential candidate of Architecture Description Language for the formal specifications of software architecture models. The class constructs in TCOZ are well suited for component declaration. The communication interfaces, i.e., channel, sensor and actuator, act as implicit connectors for modeling the

communications between components. The network topology is used for defining the configuration of the system. All these features may provide a more consistent and flexible way of specifying software architectures. Furthermore, in this paper we also demonstrated the verification of architecture properties via formal reasoning. We combined and extended both state-based and event-based proof systems of Object-Z and TCSP for verifying TCOZ specifications. Complex system properties are decomposed into state and event related properties and proved respectively. In summary, the paper demonstrates that integrated formal modeling techniques (i.e. TCOZ) can be a good candidate for modeling and verifying various level descriptions of software architectures.

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