POSAR: A FLEXIBLE POSIT ARITHMETIC UNIT FOR RISC-V

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1 Motivation and Research Questions

Motivation
- IEEE 754 floating-point is widely-used in both HPC and ML applications.
- IEEE 754 is error-prone and different implementations may produce different results [1].
- Posit [2] is a new representation for real numbers which is flexible by providing a variable bit-size for both the fraction and exponent, thus representing small numbers more accurately.

Research Questions
- Is posit more efficient than single-precision, 32-bit IEEE 754 (FP32)?
- What is a good trade-off between accuracy and time-energy efficiency when employing low bit-size posit?

2 Approach

POSAR – Posit Arithmetic Unit

- Implemented in Chisel language
- Integrated into Rocket Chip
- Using RISC-V F extension
- Evaluated on Arty A7 FPGA

Source code: https://github.com/sdcioc/PositChisel

3 Evaluation

- FP32 vs. Posit(32,3) – Posit16 or P32
- Posit(16,2) – Posit16 or P16
- Posit(8,1) – Posit8 or P8

- 10 benchmarks, 3 levels (benchmark complexity)
- Accuracy (number of accurate digits after the decimal point)
- Efficiency (number of cycles)
- FPGA Resources
- Energy

4 Summary

- Posit(8,1) exhibits low accuracy and it cannot replace FP32 in common HPC and ML applications.
- Posit(16,2) exhibits good accuracy for ML workloads, while using less FPGA resources (13-47% less) and less energy (2% less) compared to FP32.
- Posit(32,3) exhibits the same or better accuracy compared to FP32 but needs more FPGA resources (30% more) and more energy (up to 6%).

References