

CIDR'26

# Hash Joins Meet CXL: A Fresh Look



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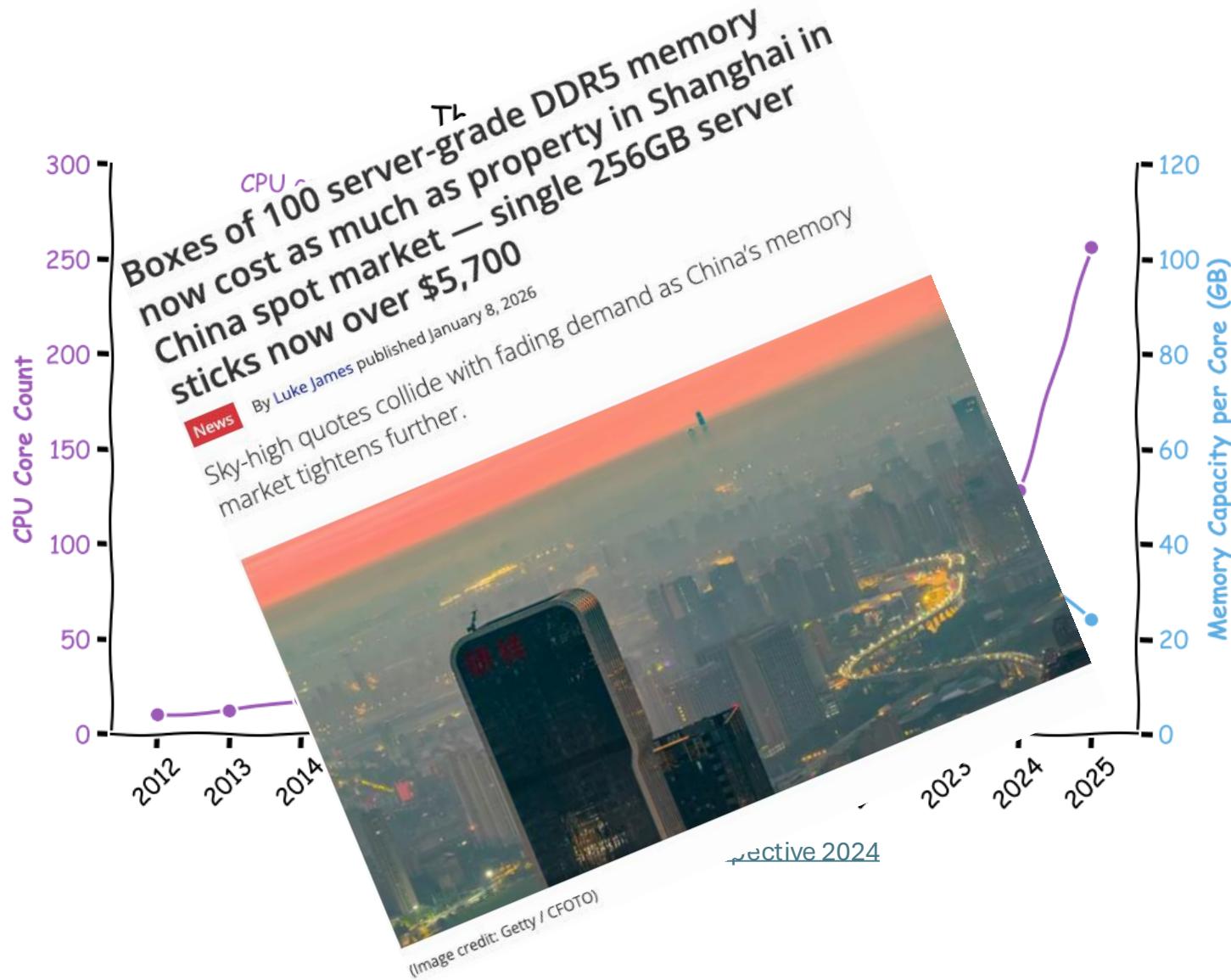
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# The Memory Scaling Wall



## Current Dilemma

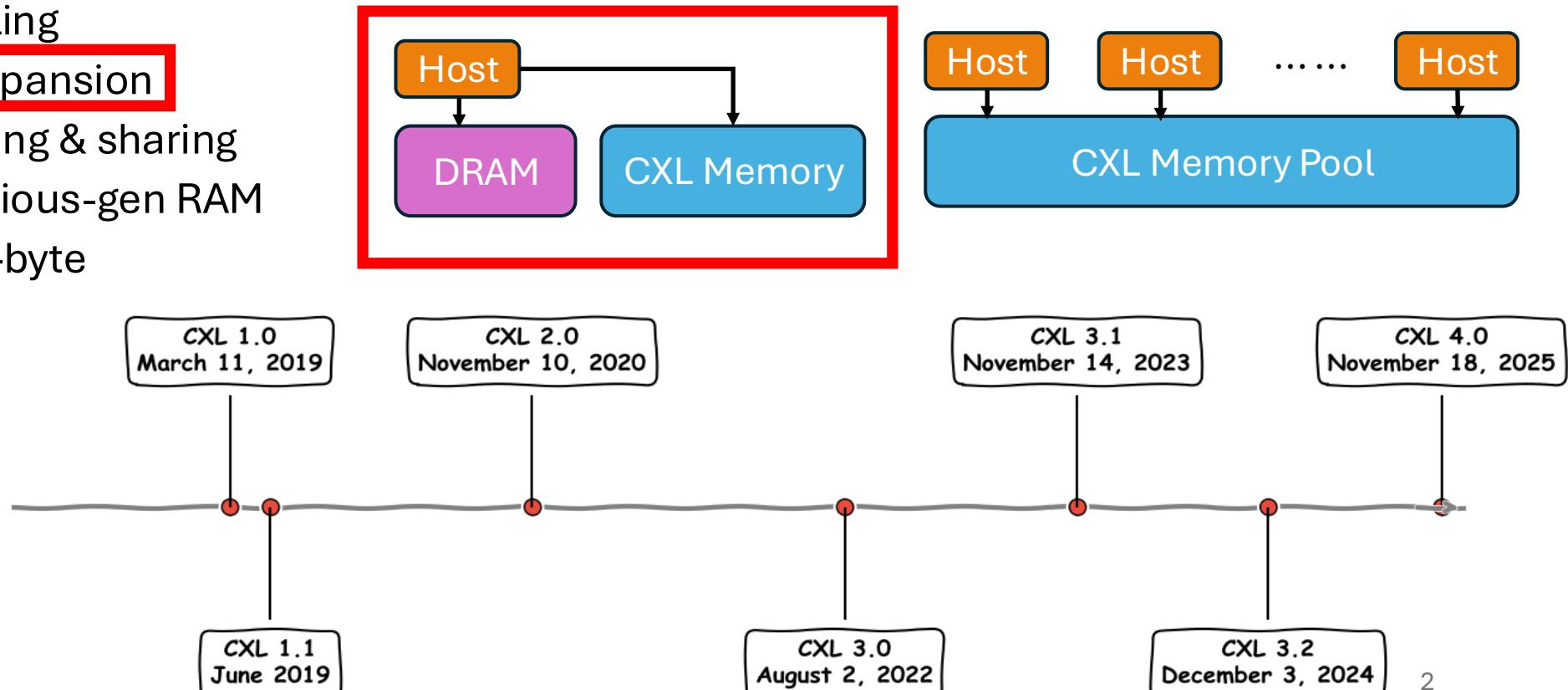
- Limited capacity-per-core
- Declining bandwidth-per-core
- Rising memory provisioning cost

# The CXL Memory Tehchnology



## CXL memory enables

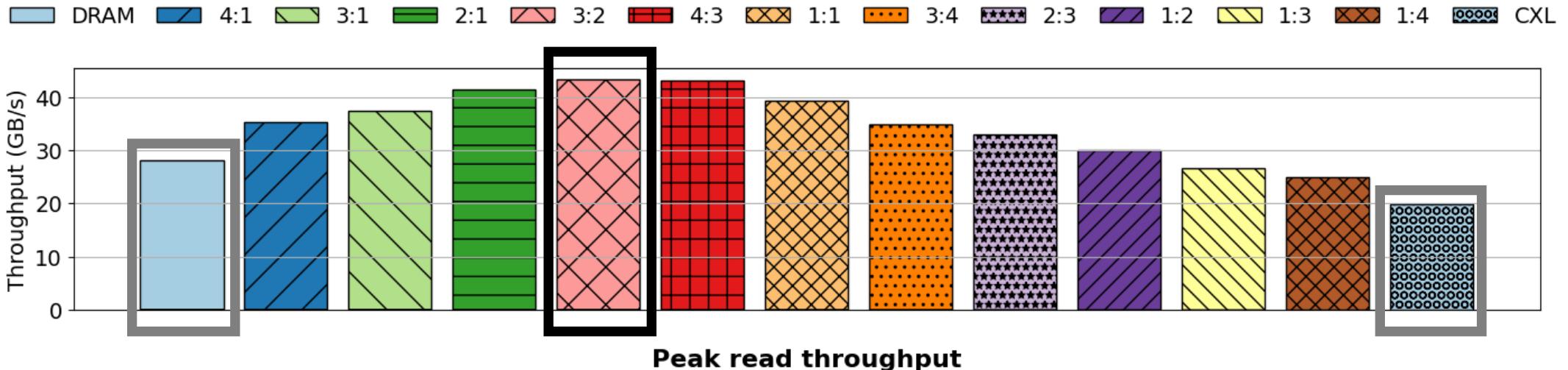
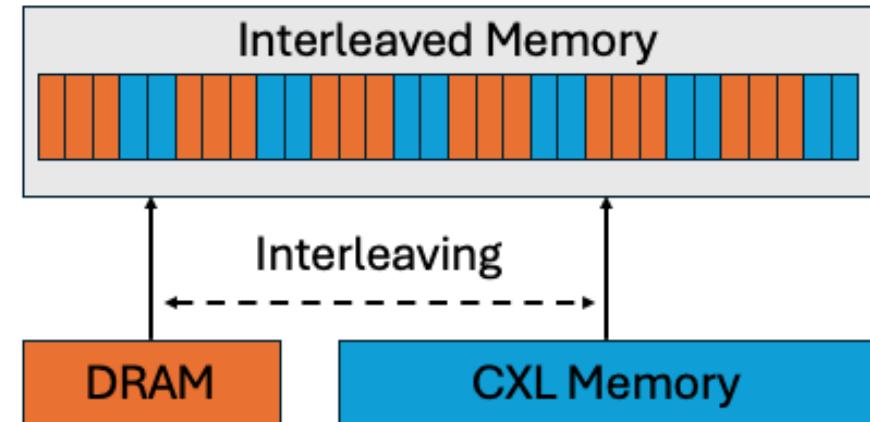
- Cache-coherent PCIe access
- Capacity scaling
- **Bandwidth expansion**
- Memory pooling & sharing
- Reuse of previous-gen RAM
- Low cost-per-byte
- .....



# Memory Interleaving

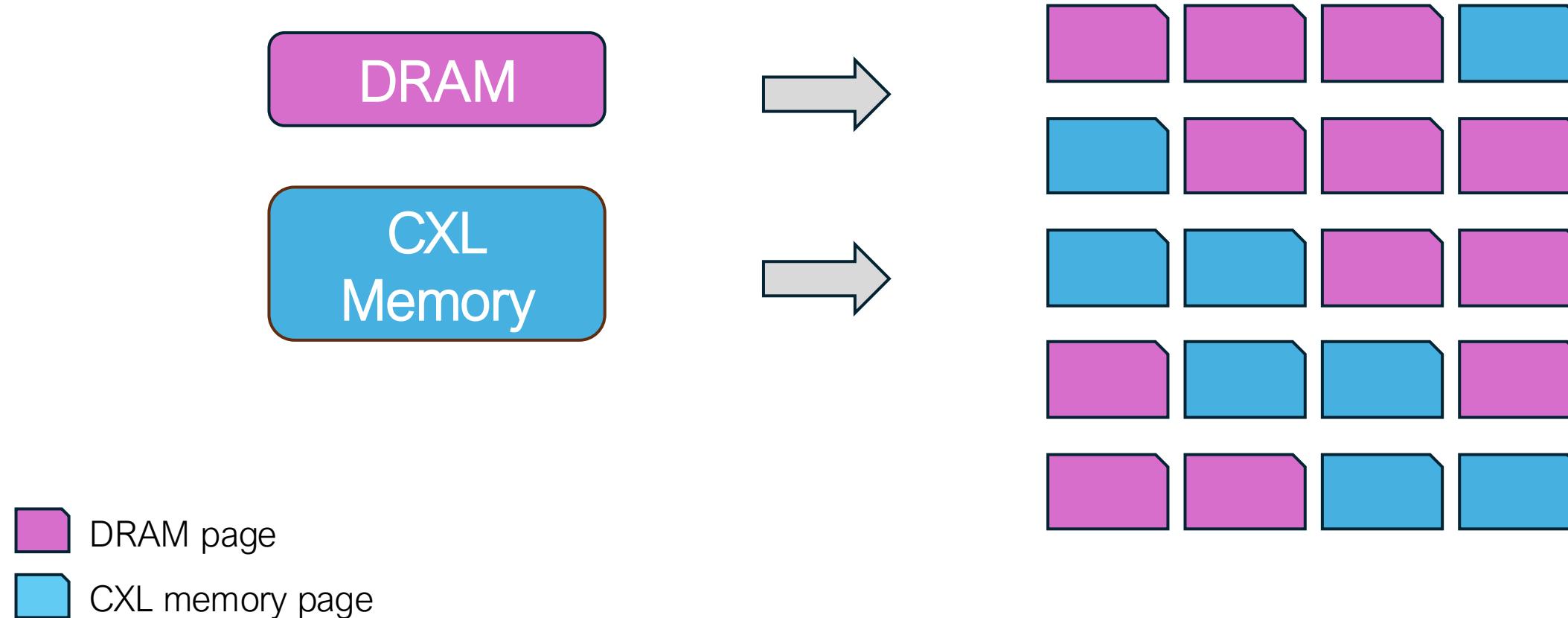
## CXL compared to local DRAM

Capacity		Larger
Latency		Higher
Bandwidth		Lower



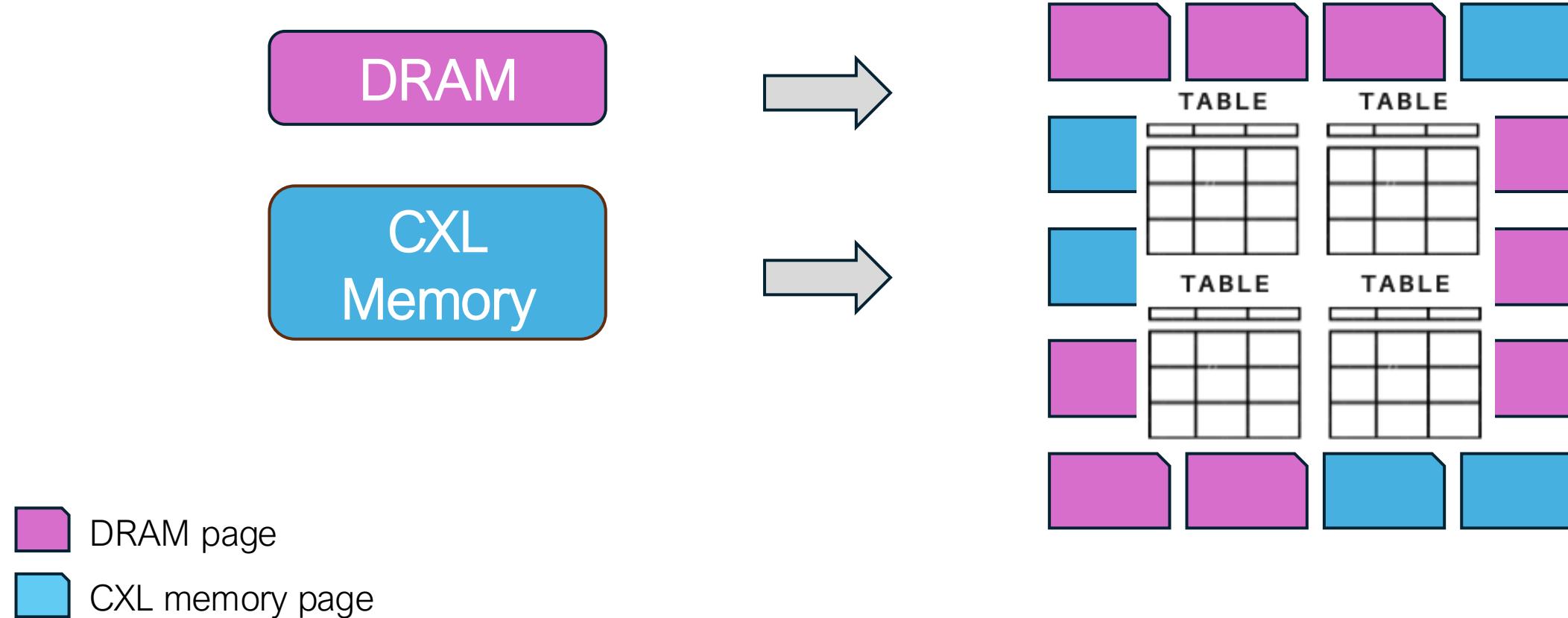
# The Status Quo Approach

Step 1 — create an interleaved memory tier



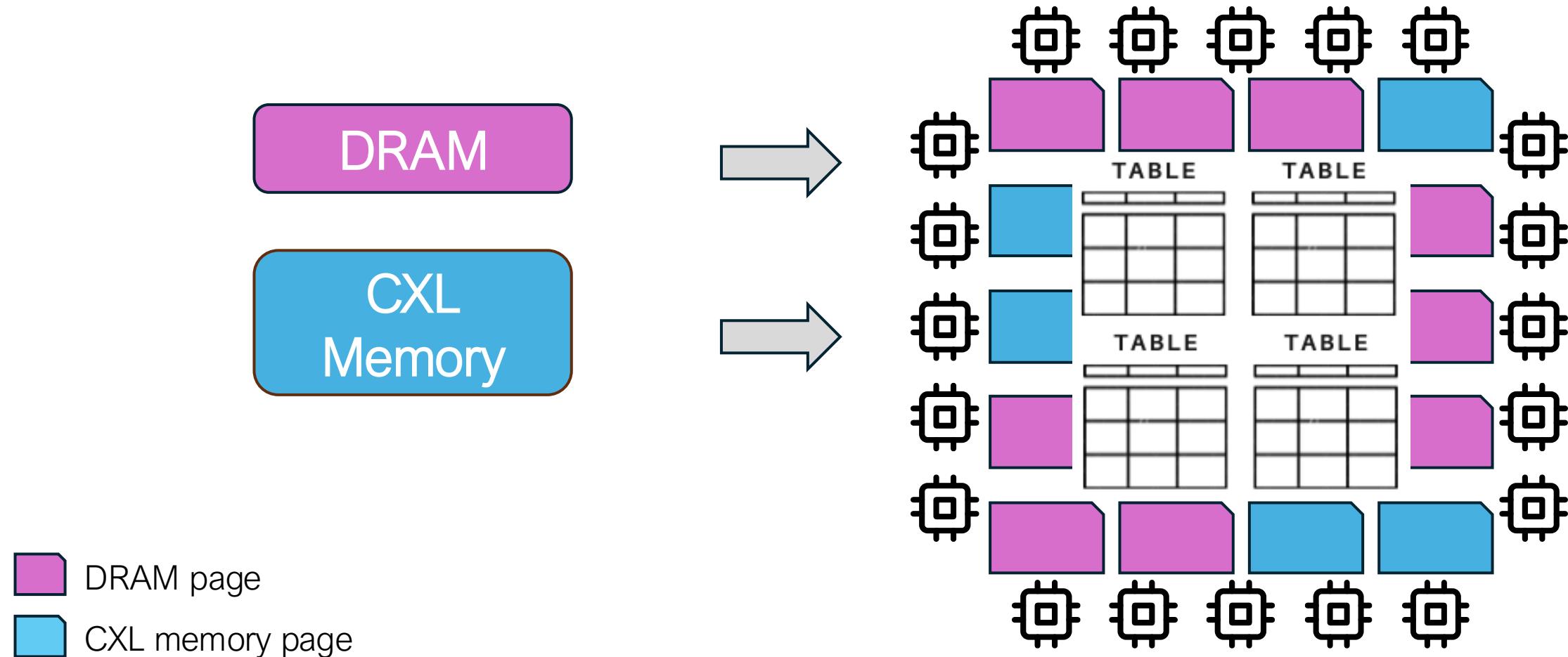
# The Status Quo Approach

Step 2 — relocate the entire workload to this tier



# The Status Quo Approach

Step 3 — run the workload in-place to maximize throughput



# The Hidden Overhead

## Total Processing Time Composition

Execution

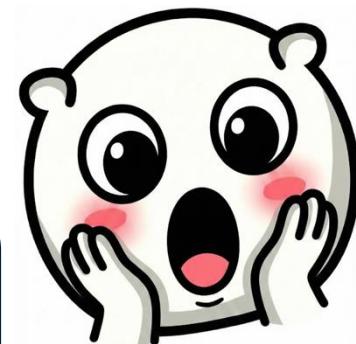
Data Movement

### The Blindspot

Most large datasets start in CXL (the capacity tier) due to capacity/economic constraints.

### The Trap

Moving overhead sometimes offsets bandwidth benefits, sometimes slower than just running in CXL!



# Shall We Stick to the Current Approach?

## The Status Quo Approach

1. create an **interleaved memory tier** (DRAM + CXL)
2. relocate the **entire workload** to this memory tier
3. run the workload **in-place** to maximize throughput



# Maybe a Better Way?

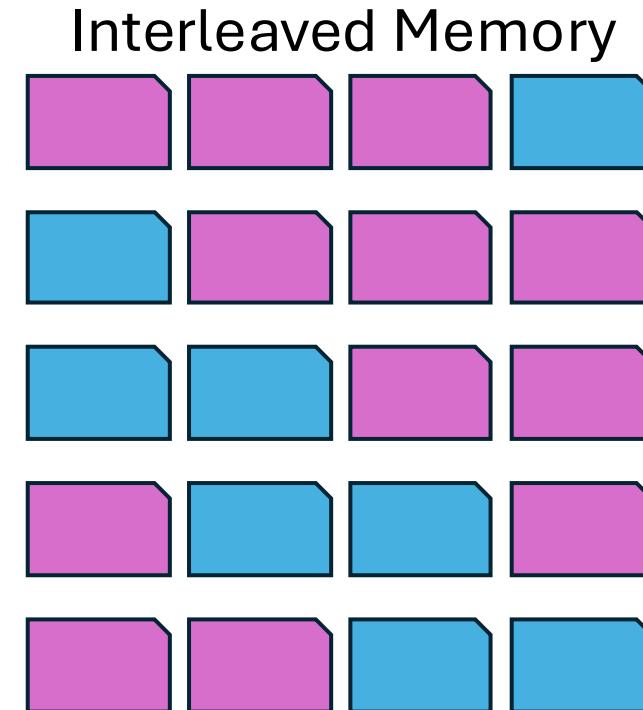
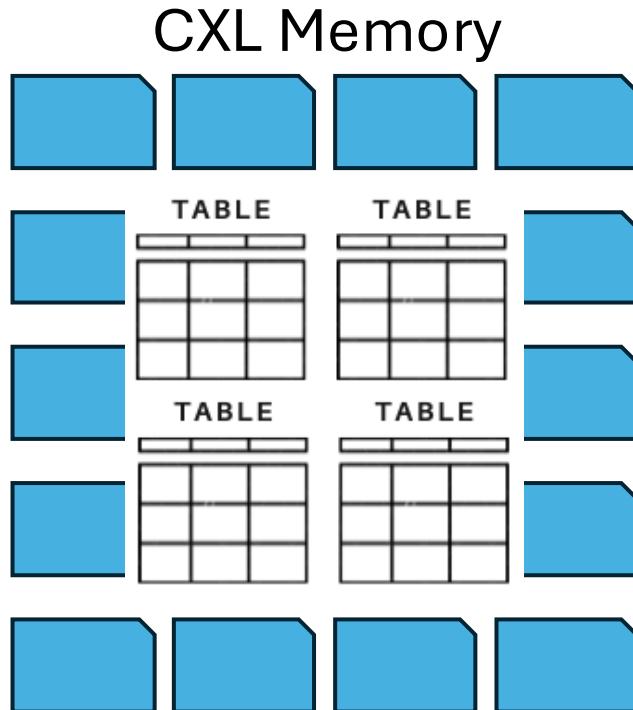
- 1. Where should we move the workload?**
- 2. How much workload should we move?**

**Reduce Data  
Movement Cost**

**Maximize Overall  
Processing Throughput**



# Data Movement Analysis: Destination



**Total Memory Traffic**

$12 \times$   $28 \times$

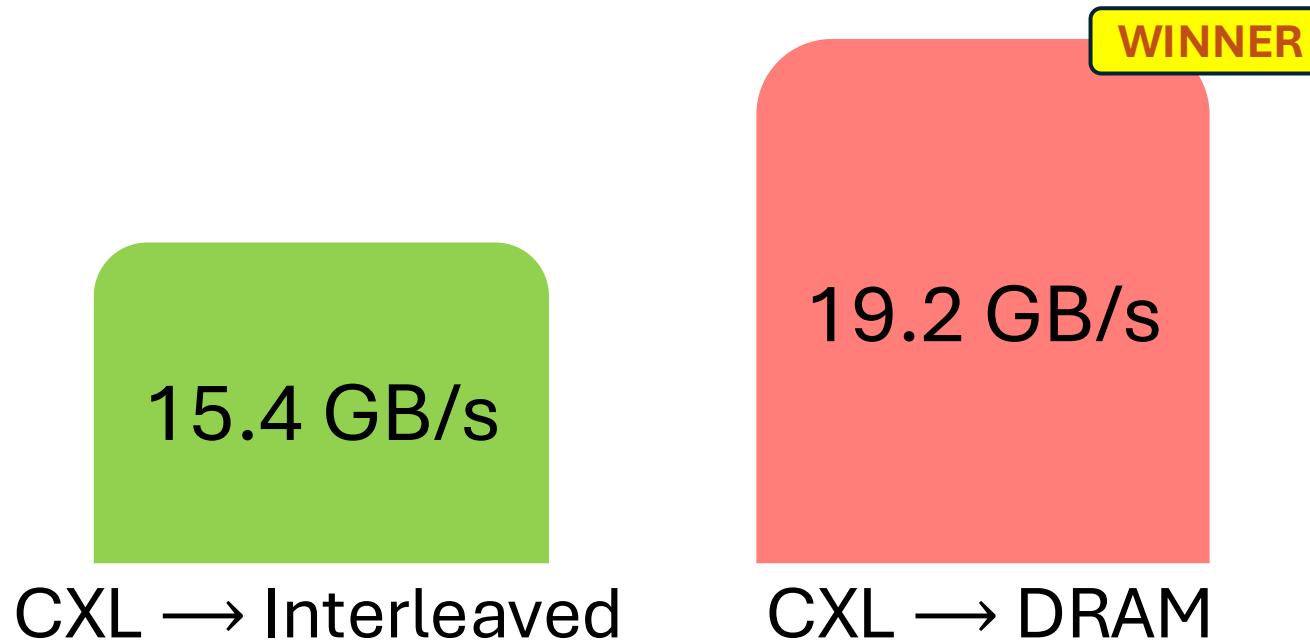
**The Fact**

: = 3 : 7

**The Goal**

: = 3 : 2

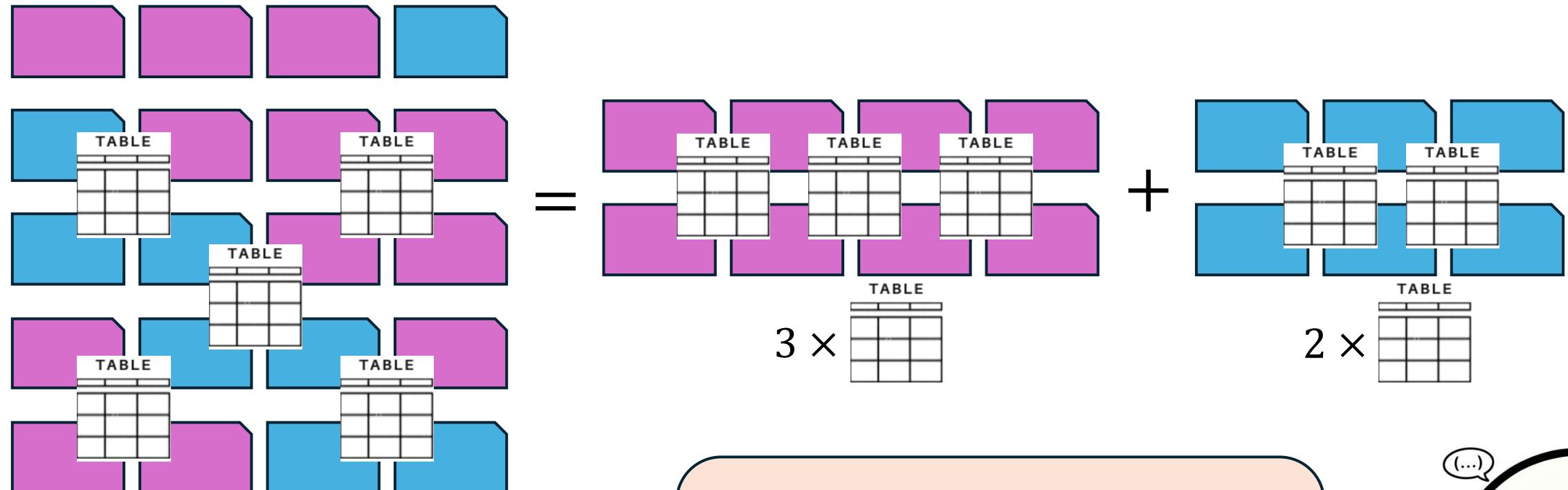
# Data Movement Analysis: Destination



**Move to DRAM for peak performance**



# Data Movement Analysis: Volume



**An Opportunity**  
High processing throughput  
with reduced data movement?



■ DRAM page

■ CXL memory page

# An End-to-End Processing Approach

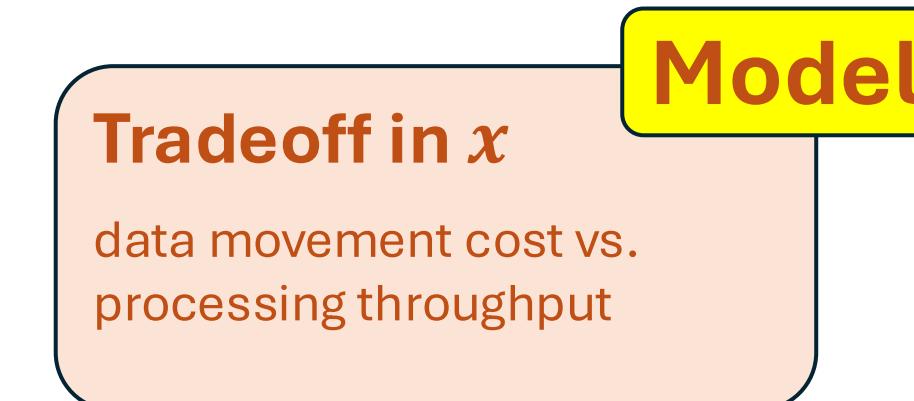
## Our Proposal

### Partial Data Movement

- **Do not move everthing**  
Avoid massive overhead of full workload movement.
- **Software-defined Interleaving**  
Accessing both DRAM and CXL for higher throughput
- **Calculate movement fraction  $x$**   
Move only optimal fraction  $x$  to DRAM;  
Leave  $(1 - x)$  in CXL memory.



Virtual “Interleaved” Tier



# Applying to Main-Memory Hash Joins

## Partitioned Hash Join (PHJ)

Bandwidth heavy: partition phase

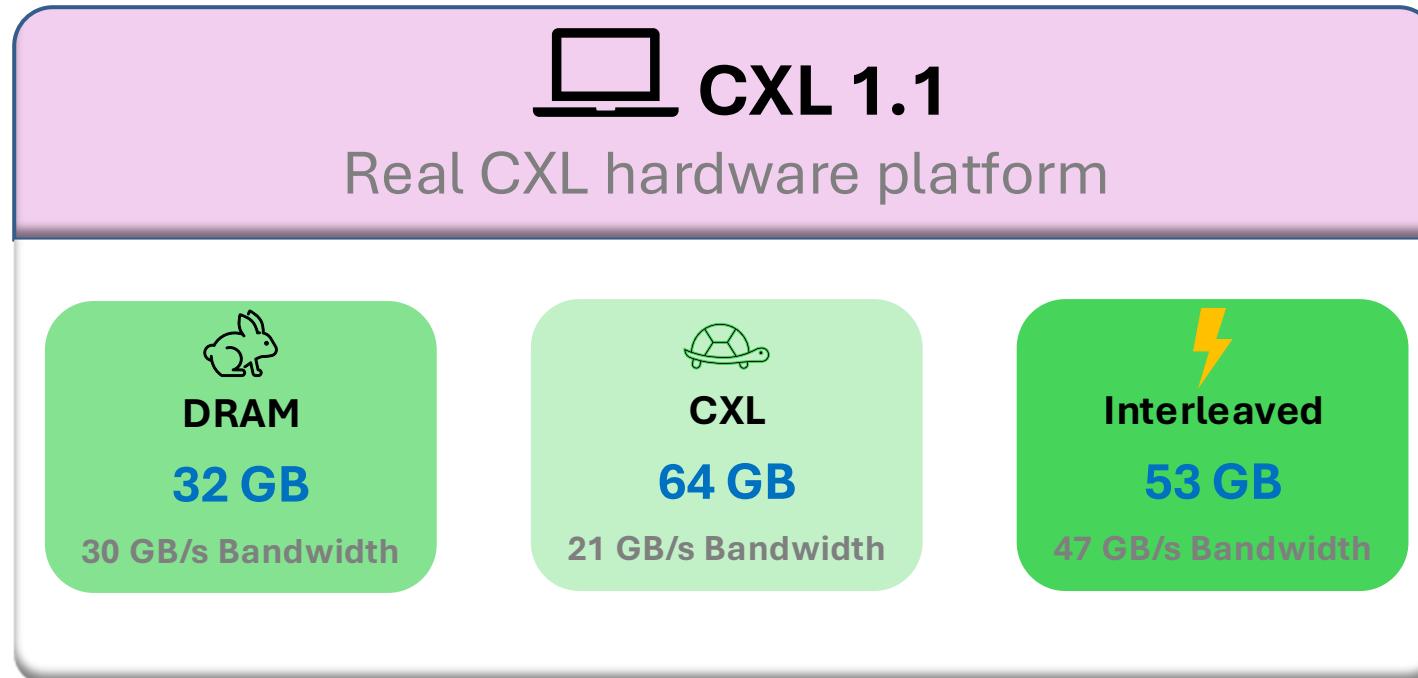
- Apply model to the **partition** phase
- Move  $x$  amount of input to DRAM
- Partition output goes to the **interleaved** tier (for maximizing **write** throughput).

## Non-Partitioned Hash Join (NPHJ)

Latency hiding: build & probe phase

- Apply model to **build and probe** phase
- Move  $x$  amount of the build side to DRAM
- The built Hash table goes to the **interleaved** tier (for maximizing **write and probe** throughput).

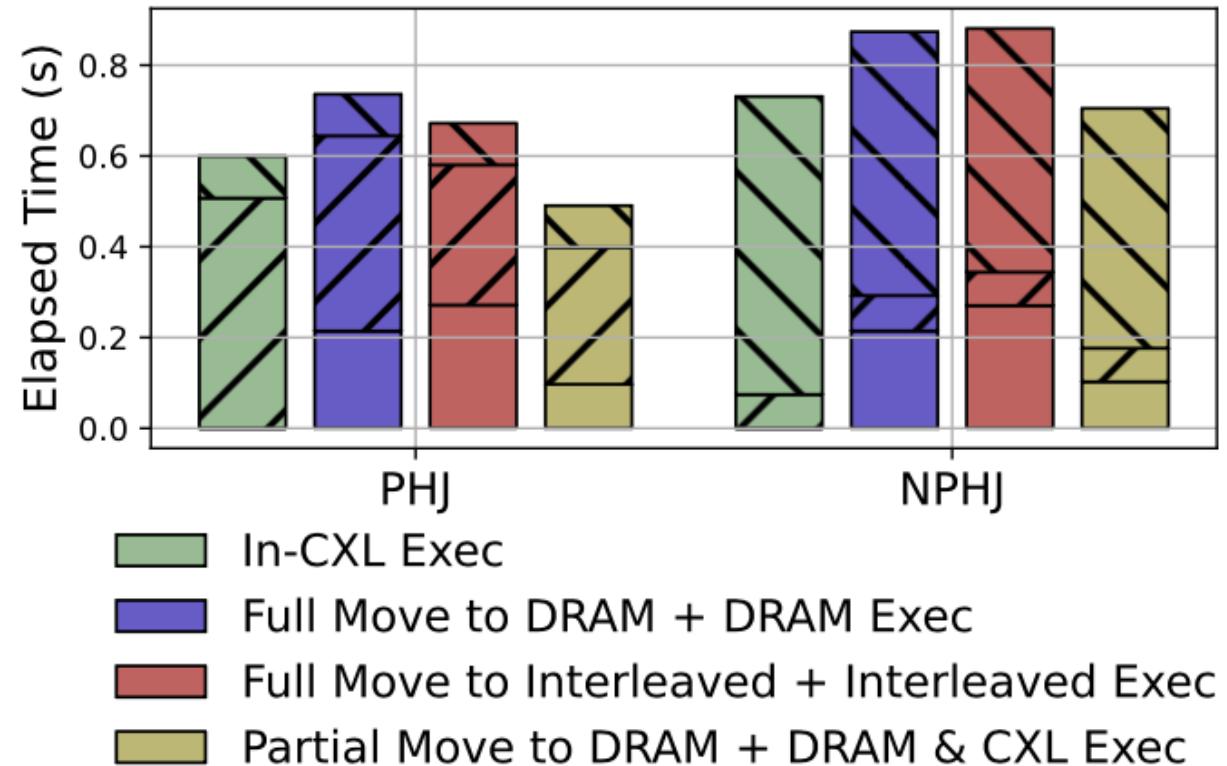
# Experimental Setup



## Workload

- Synthetic equi-join benchmark (16-byte tuples)
- Cardinality: build side **16M**, probe side **256M**

# Experimental Results



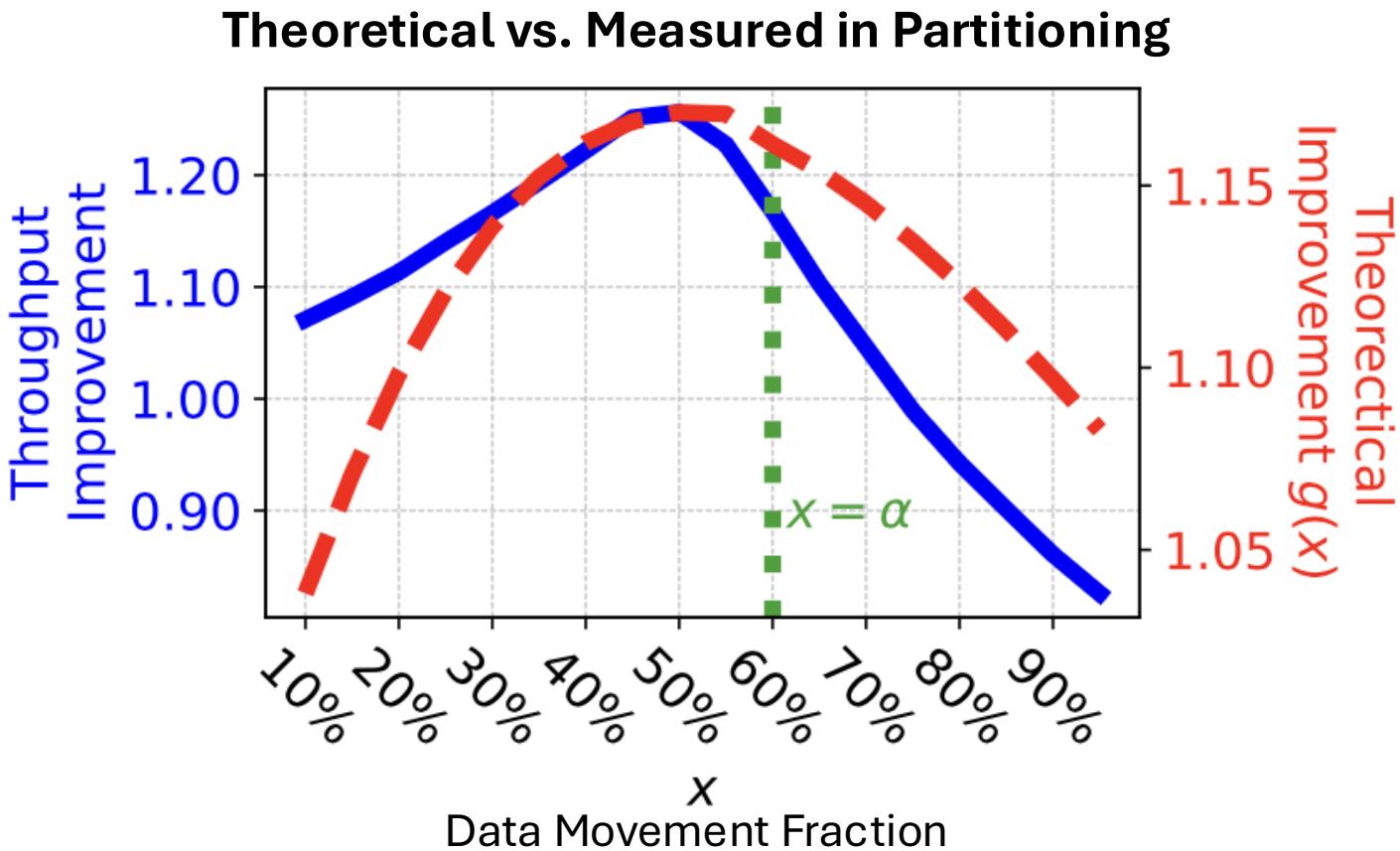
Partitioned Hash Join  
**~22% runtime reduction**  
vs. In-CXL execution

Non-Partitioned Hash Join  
**~4% runtime reduction**  
vs. In-CXL execution

“Partial move”  
beats all baselines



# Sensitivity Analysis



The model can determine the optimal data movement fraction



# Conclusion

## Takeaway

- **Interleaving  $\neq$  Answer:** data movements costs are real
- **Less can be More:** Partial movement beats full relocation
- **The Winning Strategy:** Our model finds the optimal balance

## Q & A

