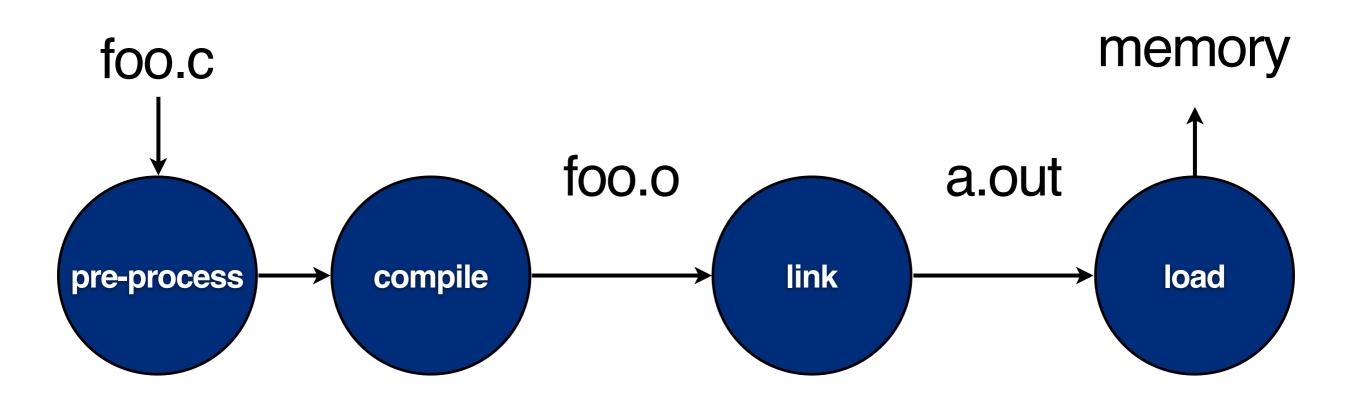
Lecture 8 Memory Management I

14 October, 2011

to build and run a program:



Memory

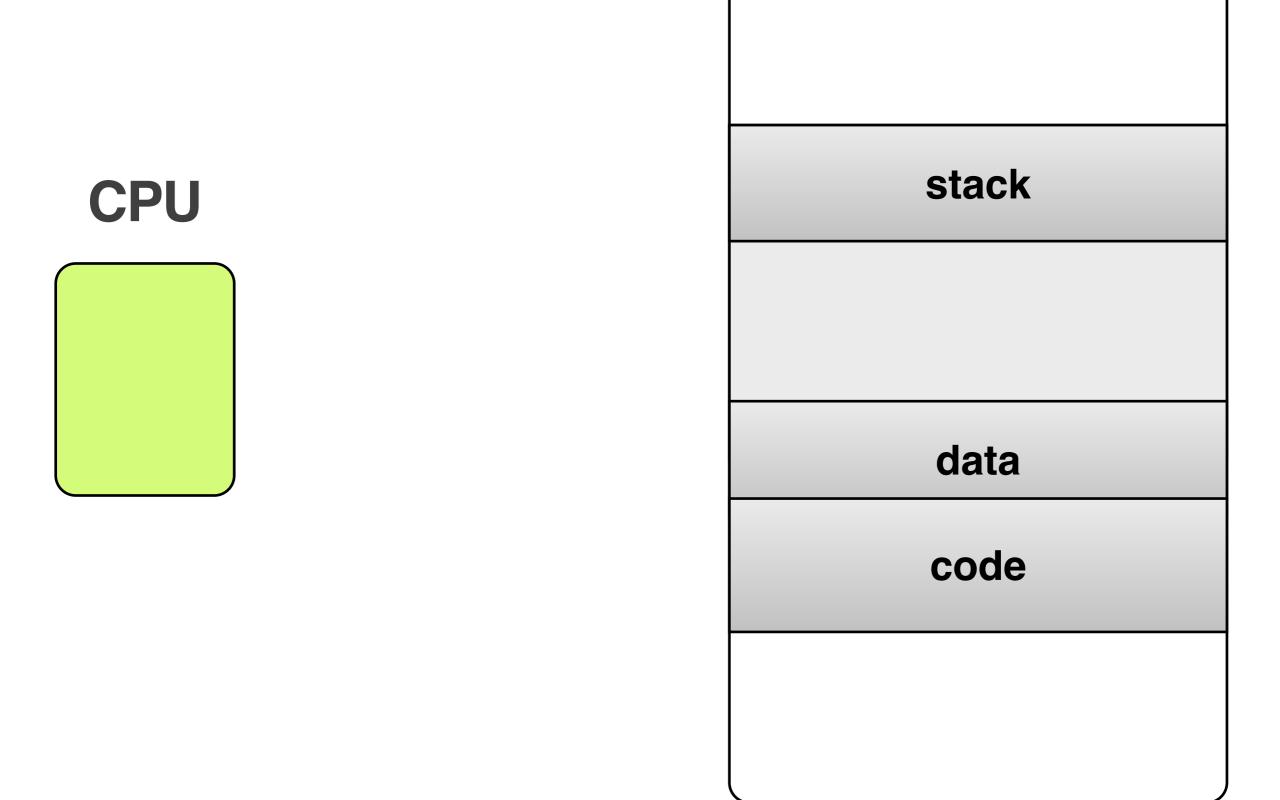


stack	
data	
code	

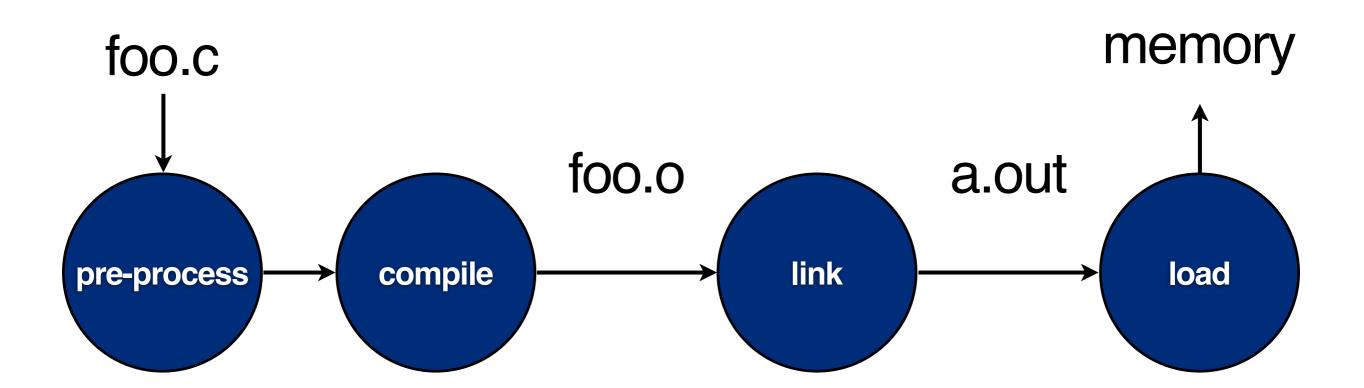
Design 1:

no address space abstraction.

processes access physical memory directly



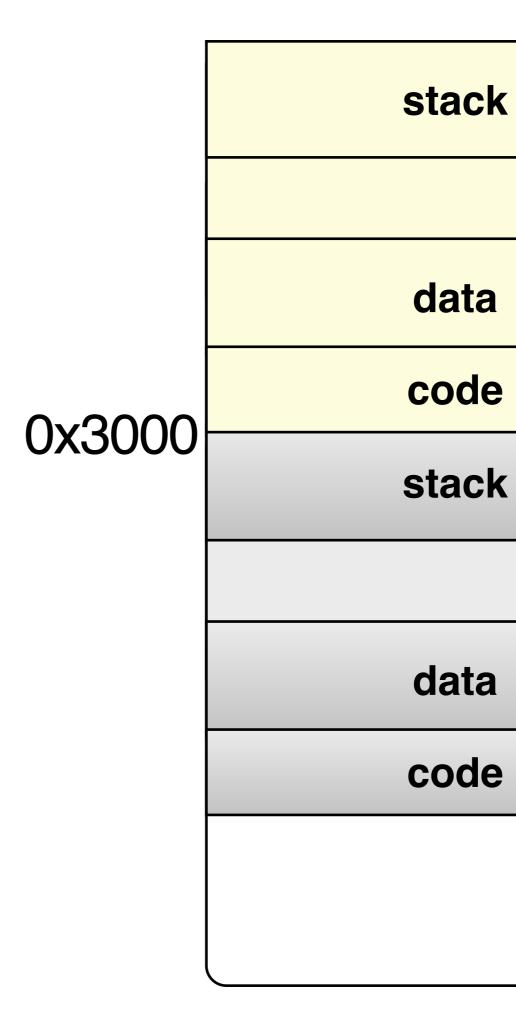
$$X = X+1;$$
 MOV R1, 0x001A
ADD R1
MOV 0x001A, R1



problem: only one process in memory at a time

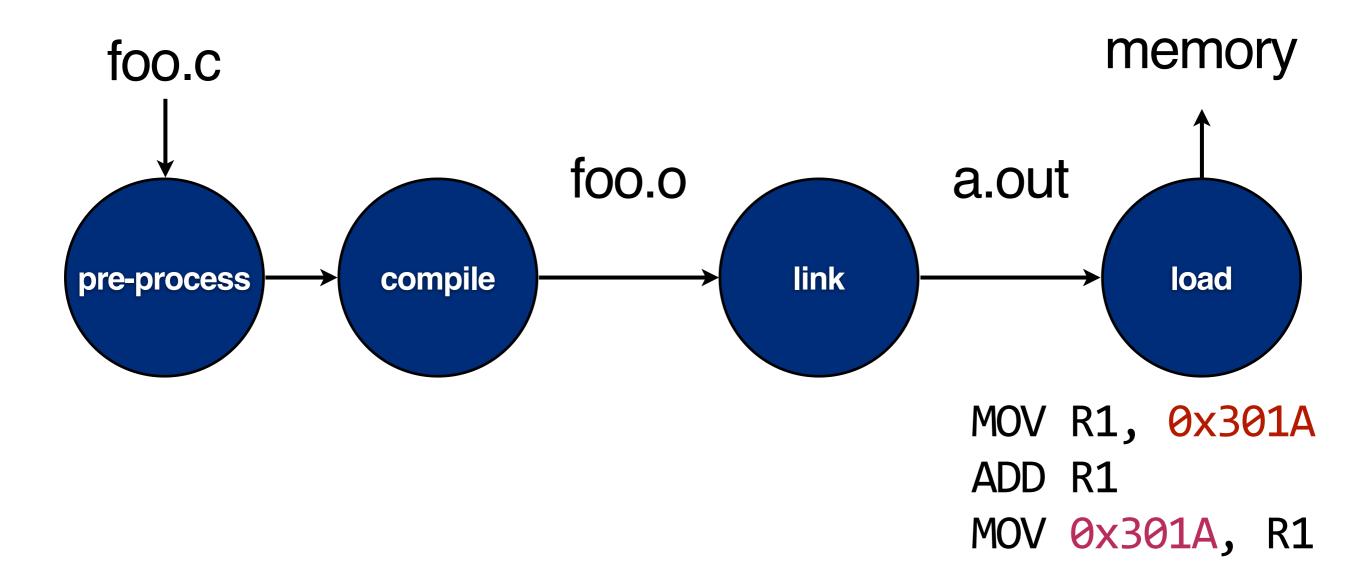
Design 2: same as Design 1, but

statically relocate process as it is loaded



CPU

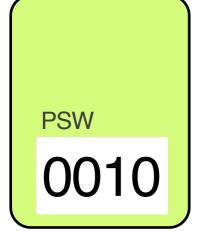




problem: no protection among processes

Design 3: memory protection through **key**-based access

CPU



key Physical Memory





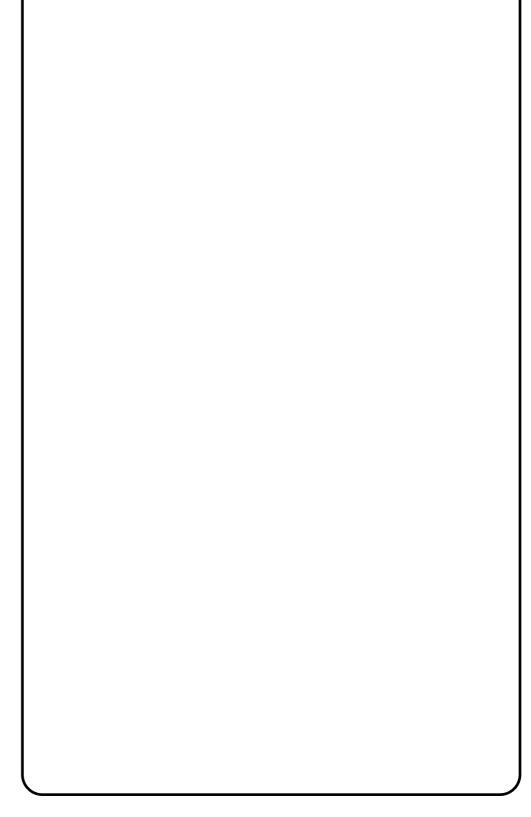


problem: loading and re-loading is slow

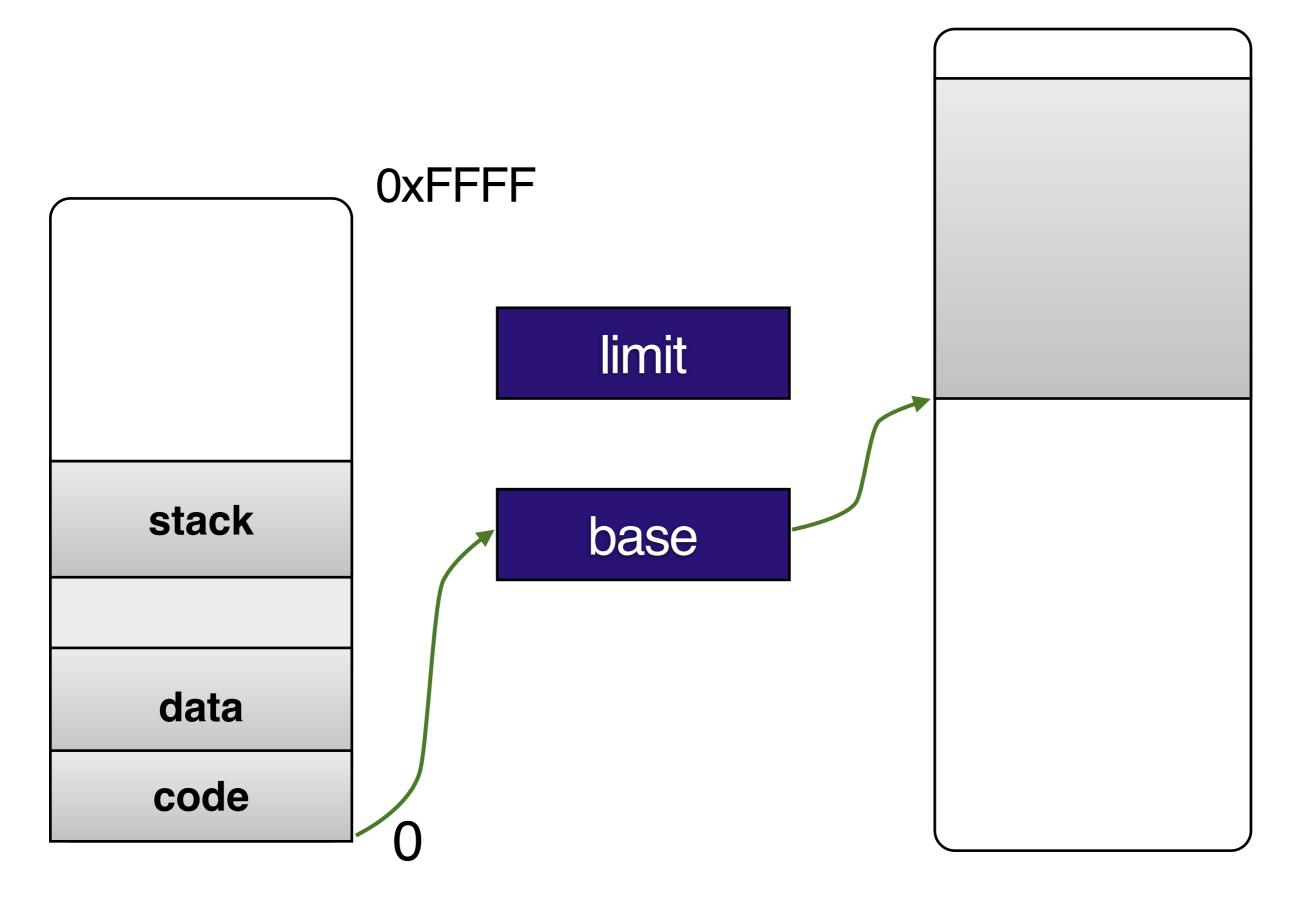
Design 4: use logical addresses computed with base and limit

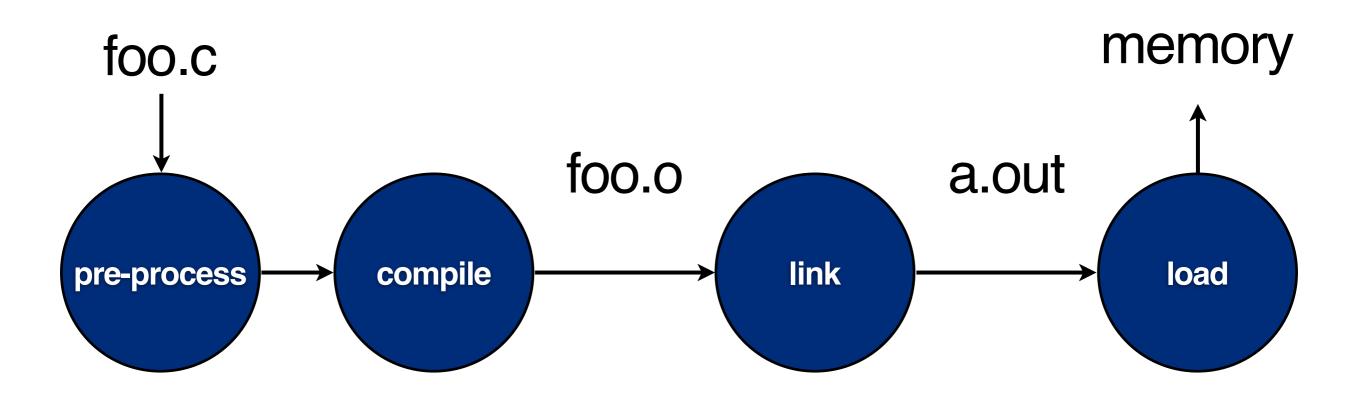
Address Space





Address Space





MOV base, 0x3000 MOV limit, 0x1000

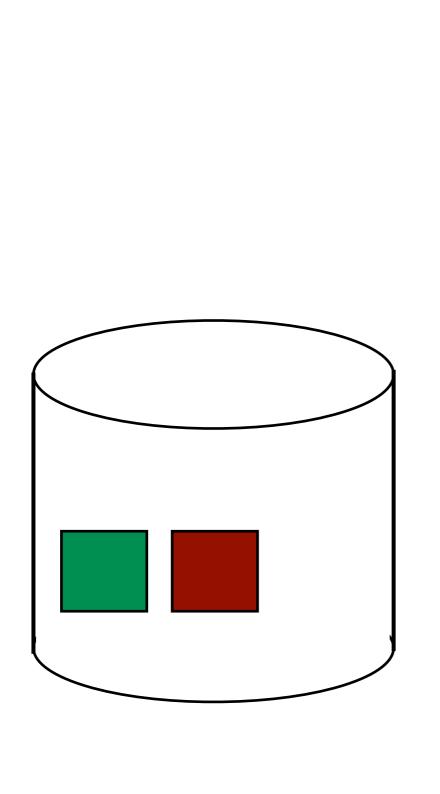
problem: add and compare for every memory reference

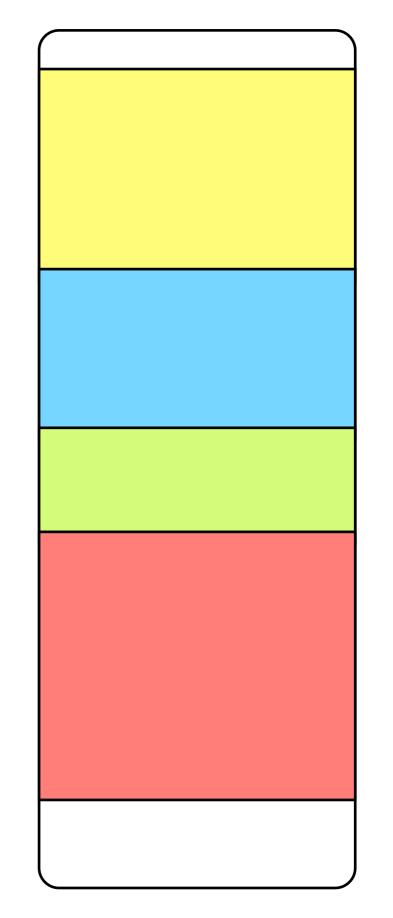
what if there is not enough memory to hold all processes?

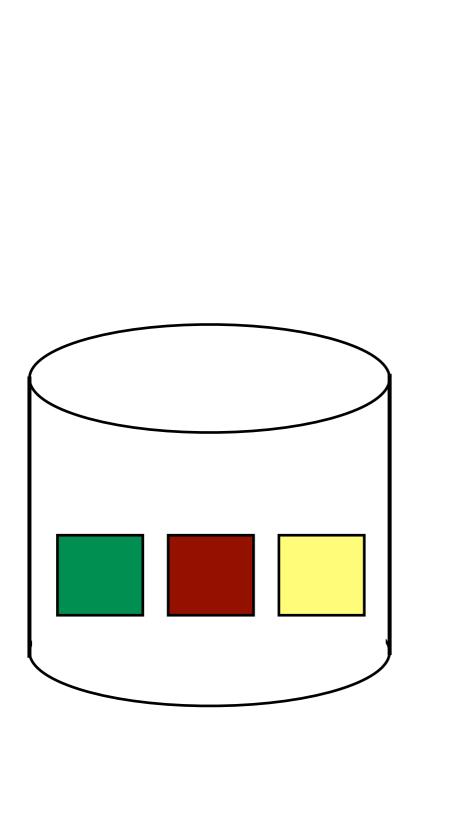
swapping

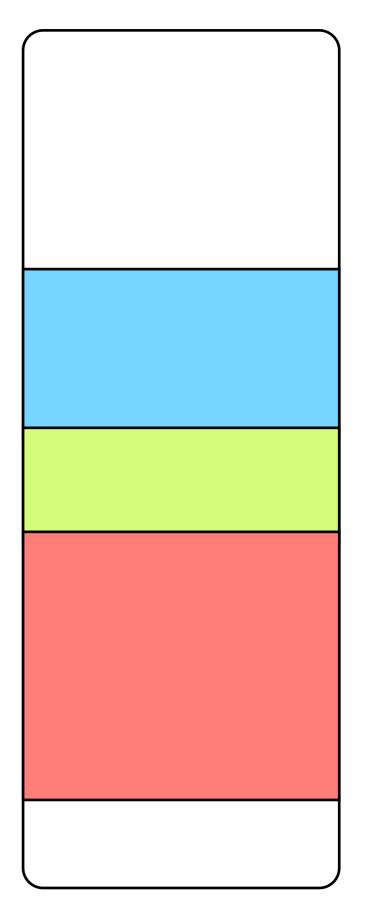
memory allocation to a process must be contiguous

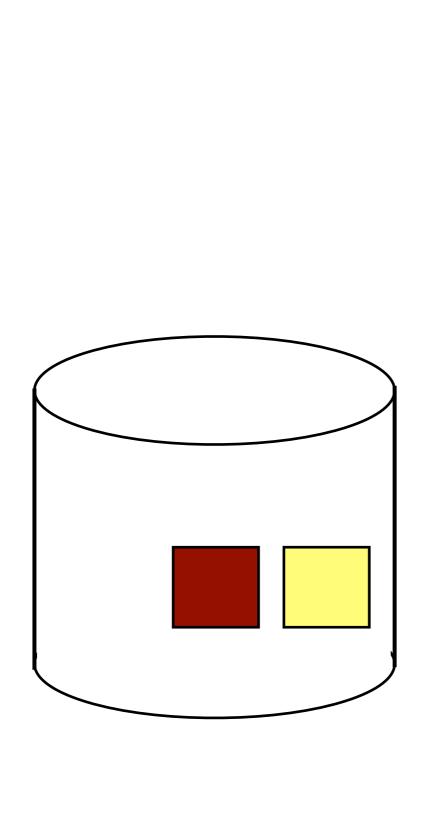
the whole process core image must be in memory

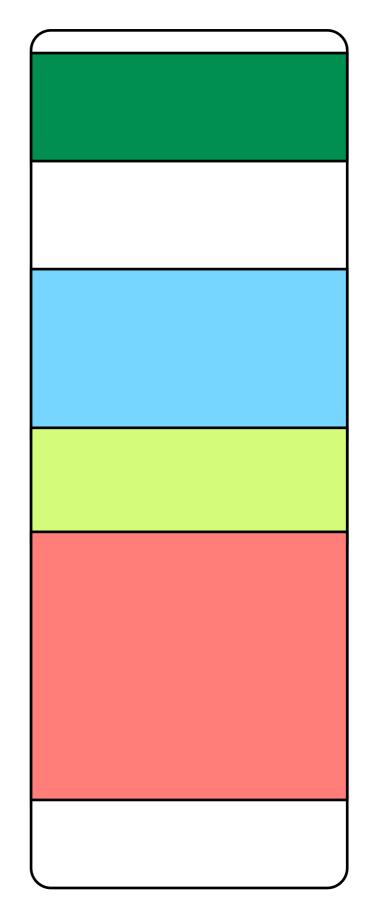


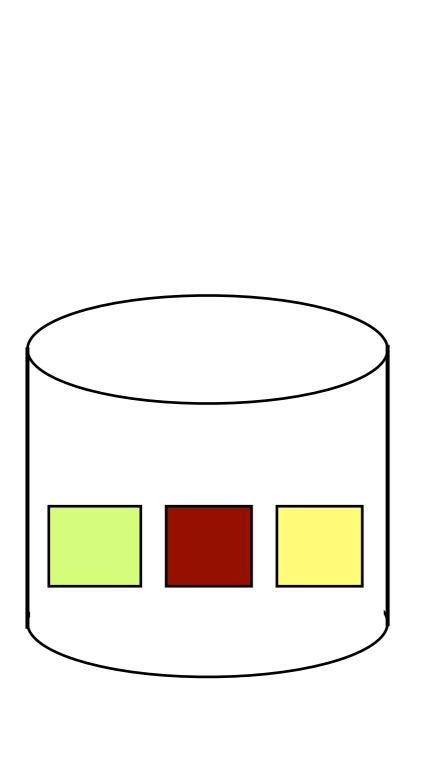


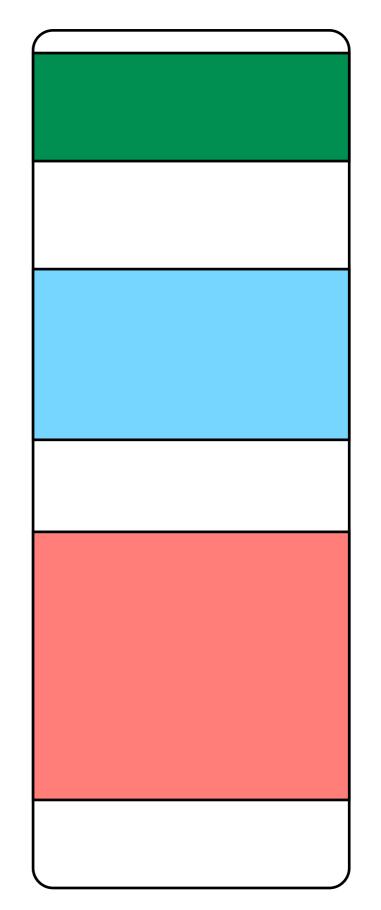






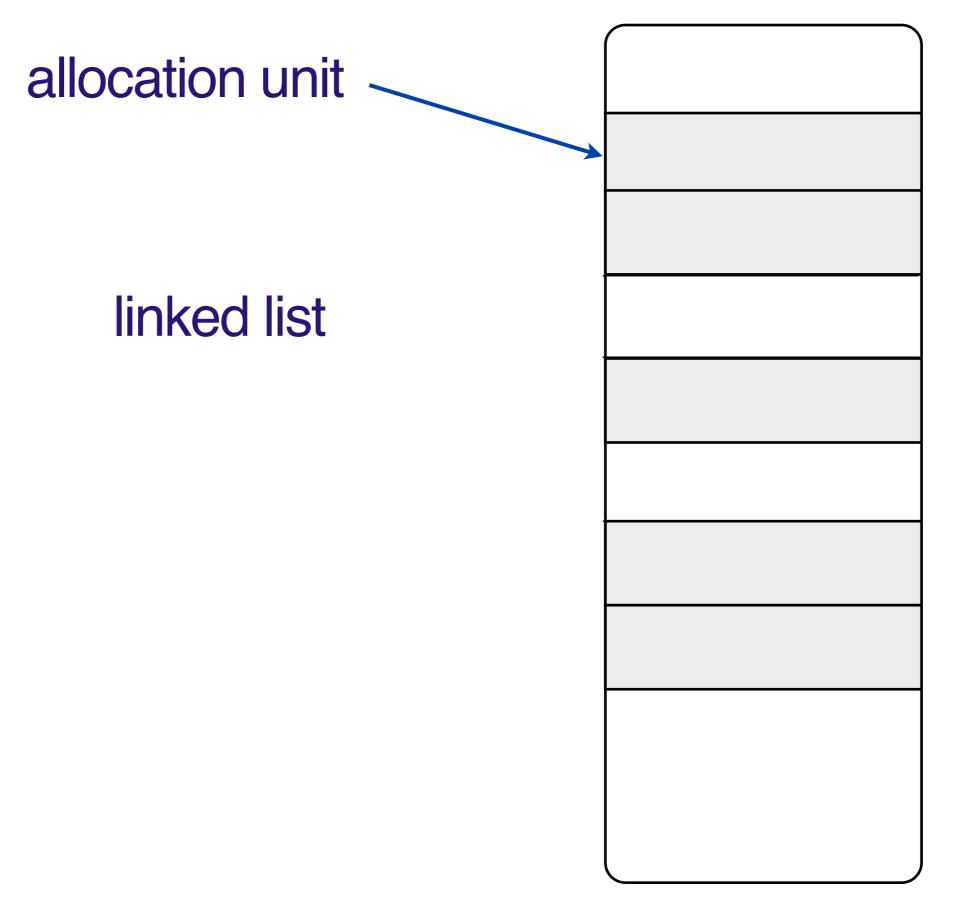






keep track of free/ occupied memory

allocation unit bitmap 01101011 ...



which hole to assign to a process?

first fit next fit best fit worst fit quick fit VS.
small
allocation units

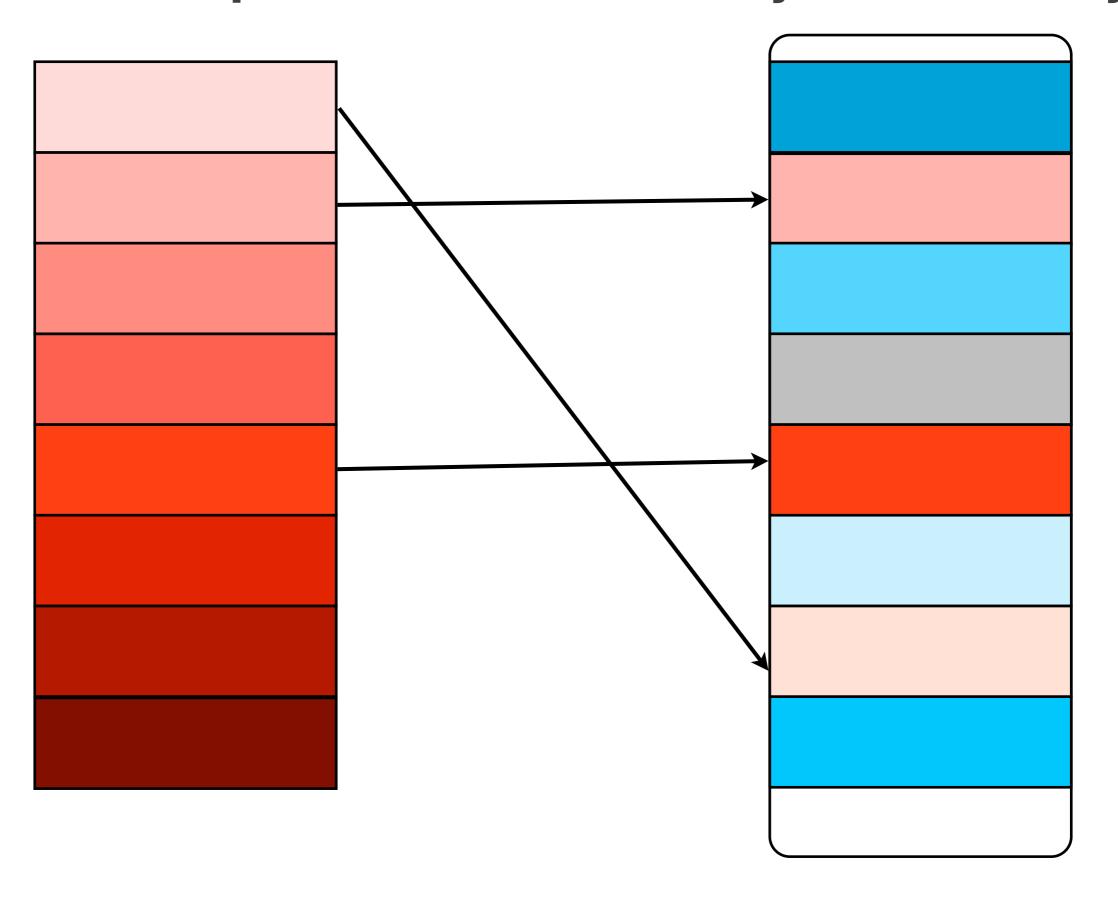
internal and external fragmentation

memory compaction removes holes, but is slow

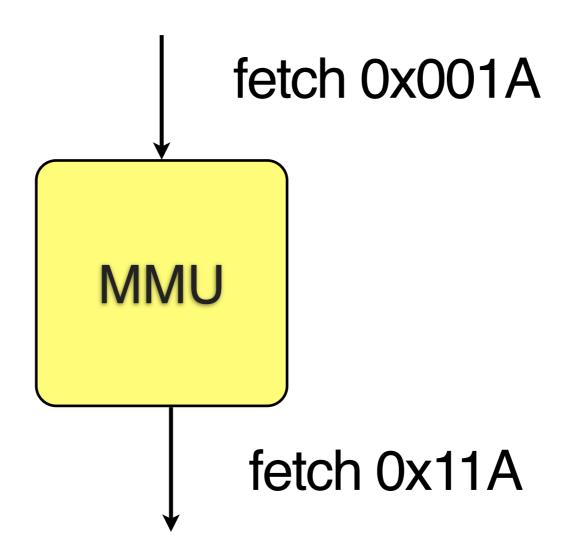
Design 5: virtual memory

organize: address space into **pages**phy. memory into **frames**

Physical Memory



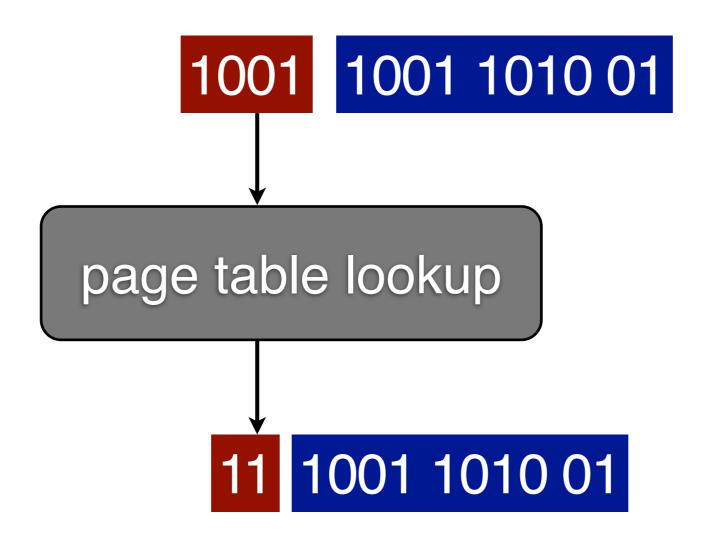
MOV R1, 0x001A



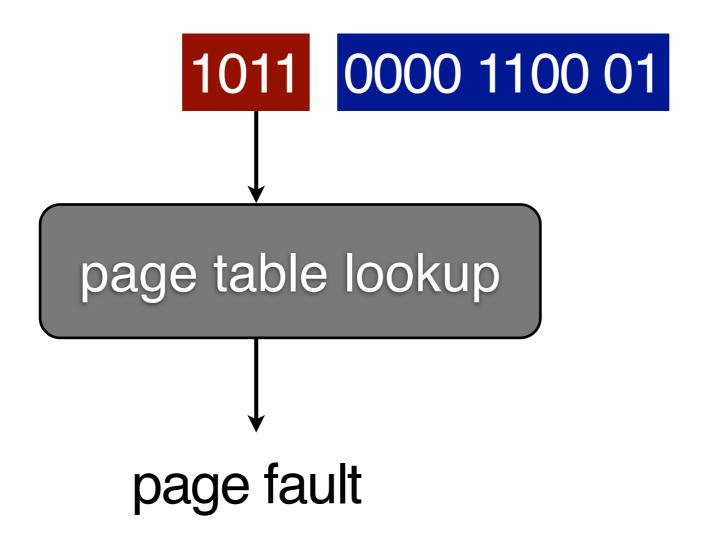
page table

page	frame	present?	dirty?	can write?	• • •
1	2	1	1	1	
2	7	1	0	0	
3	-	0	0	0	
•	•	•			

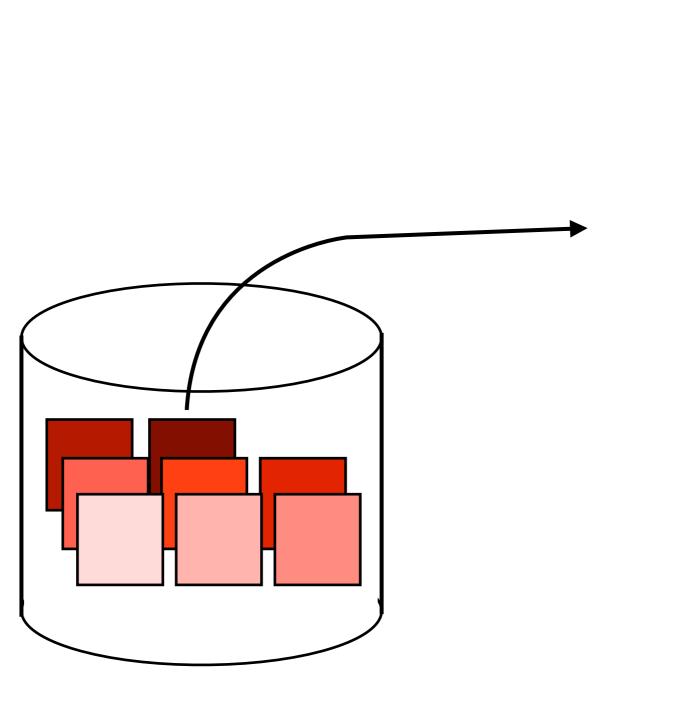
address translation

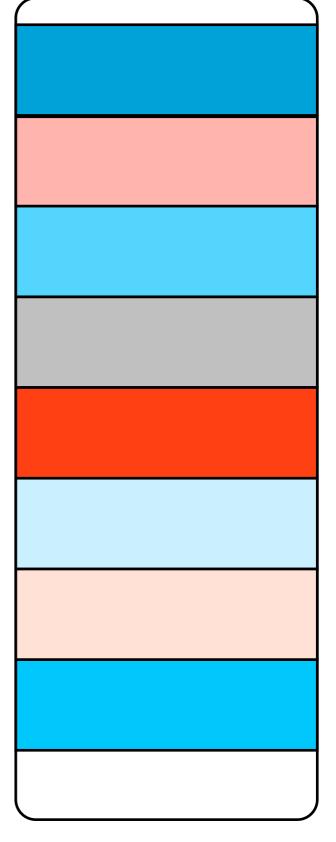


address translation



Physical Memory





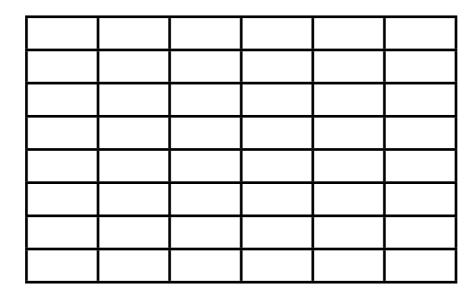
64 bit addresses4 MB page size4 GB RAM8 byte page table entry

- 1. address translation is **slow**
- 2. page table can be huge

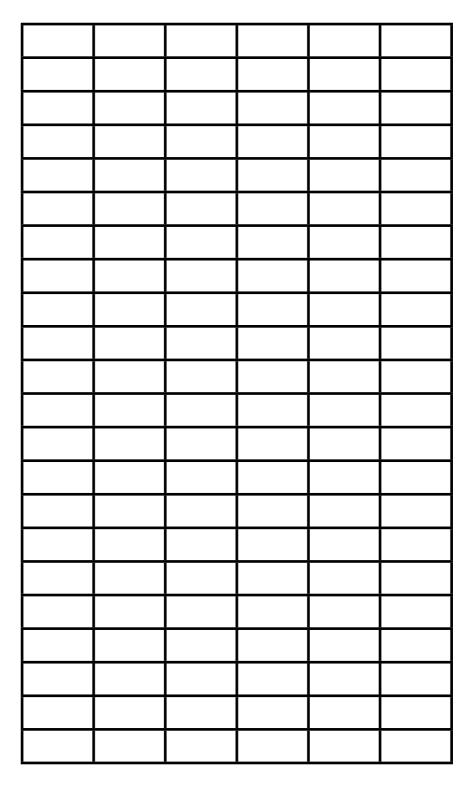
Translation Lookaside Buffer (TLB)

cache for page table entries

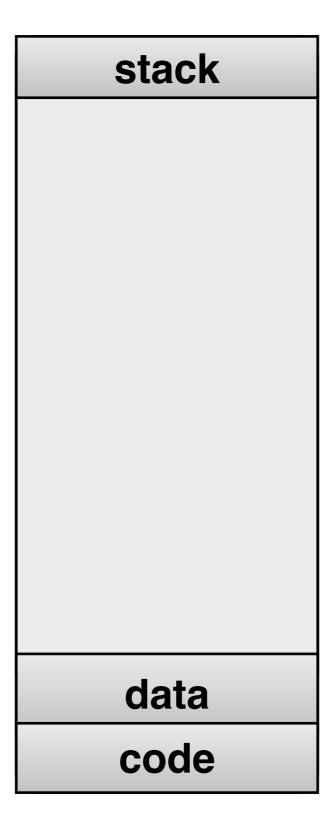
TLB (hardware)

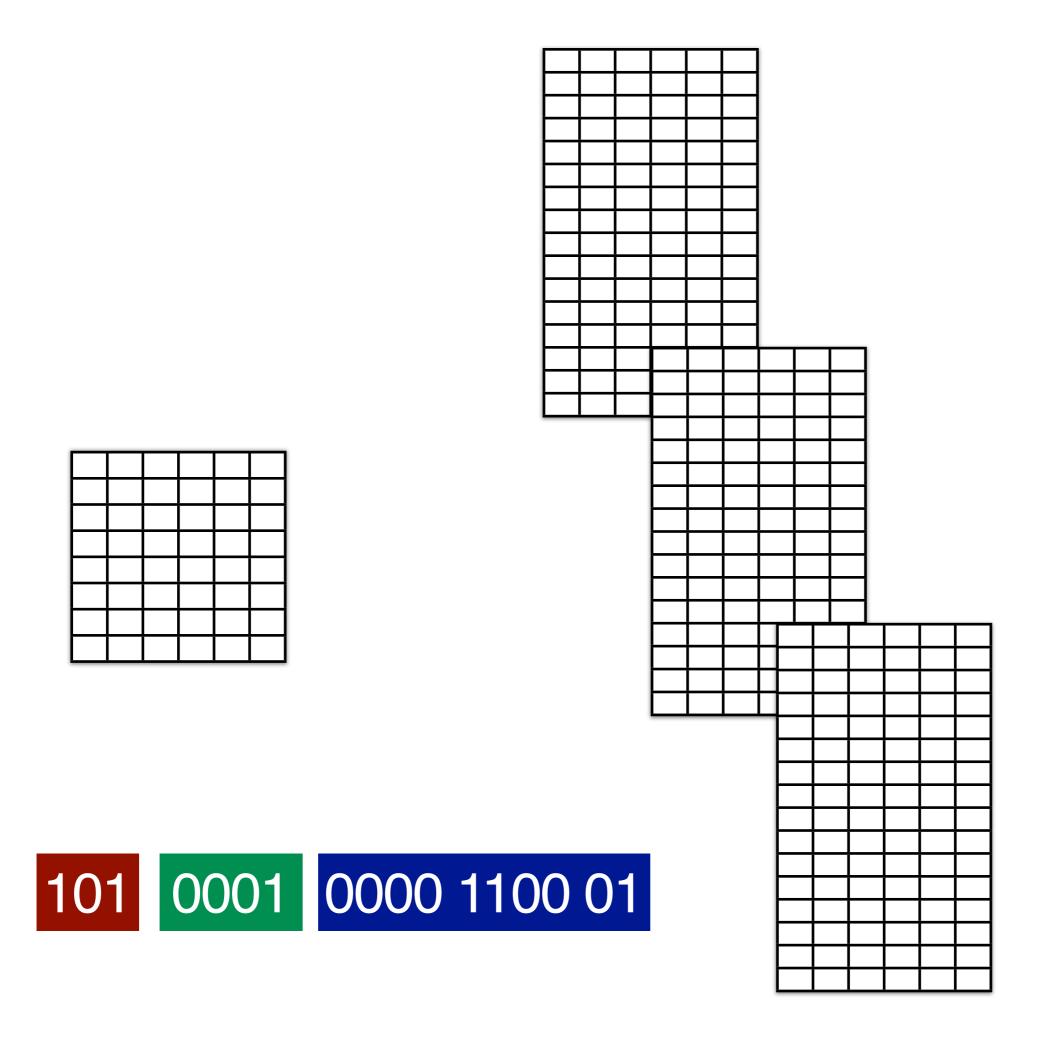


Page Table (in memory)



Hierarchical Page Table





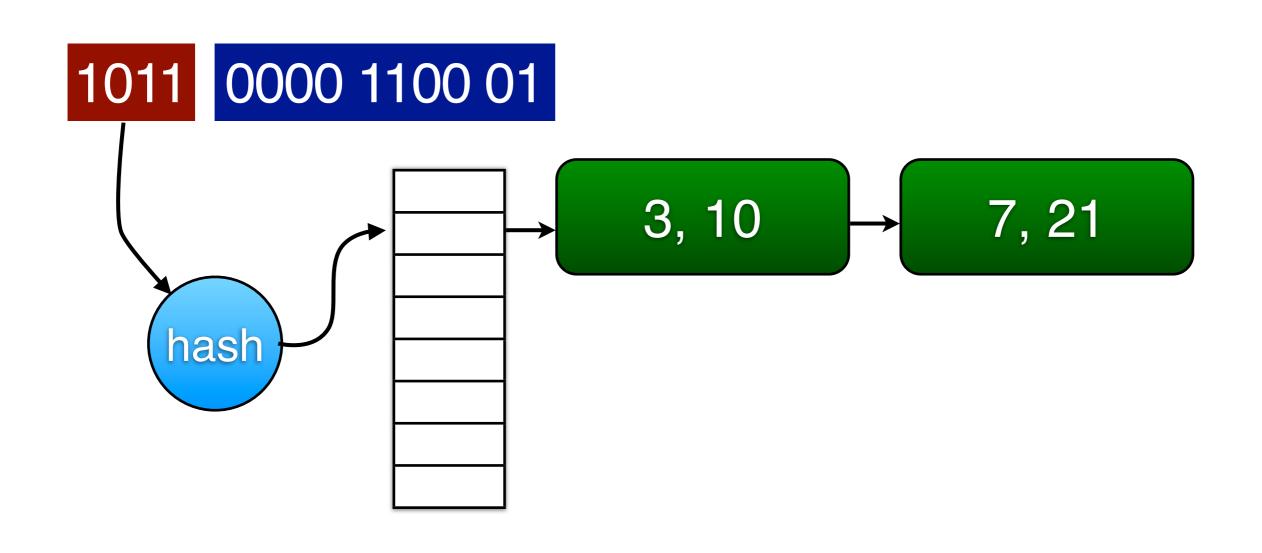
Inverted Page Table

inverted page table

frame	page	
1	2	
2	7	
3		
= =	- -	

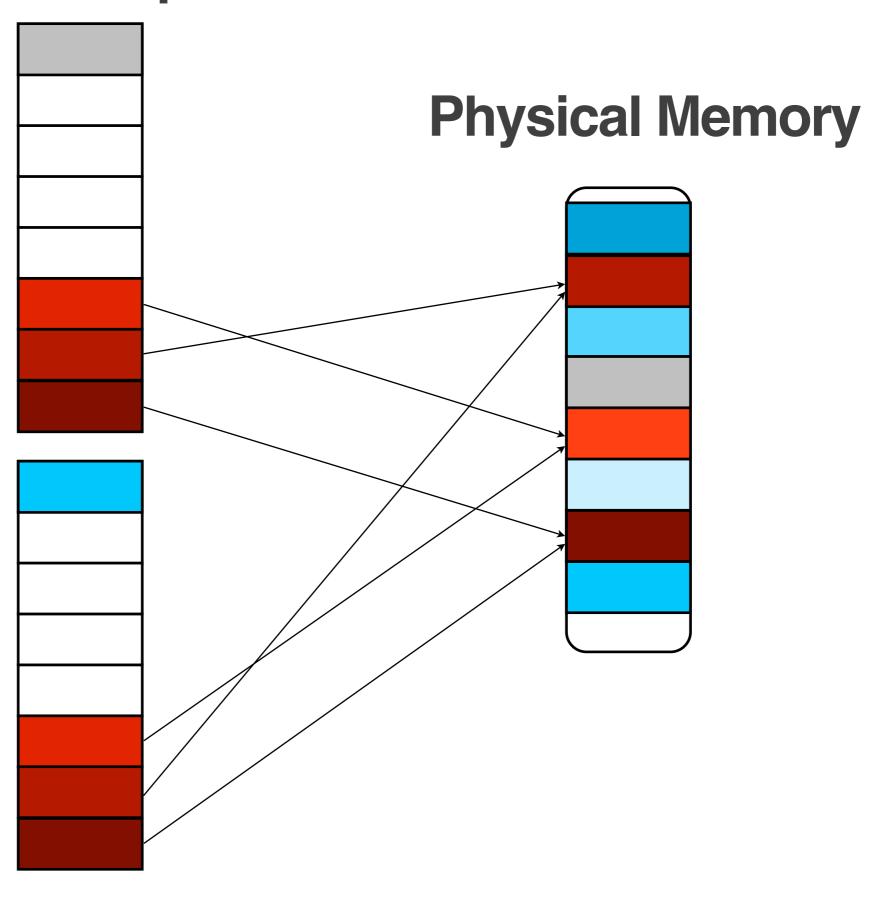
inverted page table

(using hash table)



Sharing Pages

Sharing Code (e.g, when running the same program)



Sharing Data (e.g., shared memory, copy-on-write)

